GARDA/GIRASOLE projects
The Galileo Receivers
Development

Workshop on Tools and Facilities for Galileo Receivers
ESA/ESTEC, 23 March 2006
Galileo Advanced Receiver Development Activities

- Funded by Galileo Joint Undertaking, lead by AAS-I
- Main Objectives:
  - Highlight the way for User Receivers to be “ready on the market” when the Galileo system will be operational
  - Develop a Galileo Rx SW Simulator
  - Study and assess, Receivers Core Technologies in different applications using the SW Rx Simulator
  - Develop a Mono-channel RF HW Simulator (single SV, multi frequency)
  - Develop Receiver Prototype composed of:
    - Antenna (3 band L1, E5, E6)
    - RF Front End (4 RF/IF)
    - Digital Signal Processing Channels & DSP
AAS-I:
- Project coordination
- Receiver Prototype
- Core Tech contribution

DEIMOS:
- GRANADA SW Receiver

AUDENS-ACT:
- Core Technologies

SPACE ENGINEERING:
- Mono-Channel Galileo RF Sim.

SATIMO:
- Antenna

BOOZ-ALLEN-HAMILTON:
- Rx Development Plans

CONSULTING TEAM:
- STMicroelectronics
- Politecnico di Torino
- University of Prague
- AAT
<table>
<thead>
<tr>
<th>Rx Market Category</th>
<th>Market Specific Receiver Characteristics</th>
<th>Appl.</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONSUMER</td>
<td>Single frequency (L1) Galileo+GPS, cost driven, low power, high volume, moderate performance, fast acquisition, NAV/COMM integrated devices (mobile)</td>
<td>Car, Mobile, PDA, Road applications</td>
</tr>
<tr>
<td>MASS &amp; ADVANCED</td>
<td></td>
<td>Timing, Scientific, Civil Eng., GIS, Land survey Space</td>
</tr>
<tr>
<td>PROFESSIONAL</td>
<td>Dual/Triple freq (L1, E5a/b, E6), cost driven, high performance meas, multipath mitigation, Local Elements for Diff. Corr.</td>
<td>Aviation, Maritime, Railway, Emergency</td>
</tr>
<tr>
<td>SAFETY OF LIFE</td>
<td>Dual/Triple freq (L1, E5a, E5b), req.s driven, high performance meas, high reliability, integrity, interference mitigation, certification, Integration with external sensors/systems</td>
<td></td>
</tr>
</tbody>
</table>
## Core Technologies studied for the 3 main receiver categories

<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A.1</td>
<td>A.2</td>
<td>B.1</td>
</tr>
<tr>
<td>Antenna RF Front End</td>
<td>Low/Medium</td>
<td>Medium/High</td>
<td>Medium/High</td>
</tr>
<tr>
<td>Code Acquisition</td>
<td>C.T.</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Gal/GPS</td>
<td>B/L</td>
<td>H/L</td>
<td>M/M</td>
</tr>
<tr>
<td>Code Tracking</td>
<td>C.T.</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Gal/GPS</td>
<td>B/L</td>
<td>H/L</td>
<td>M/M</td>
</tr>
<tr>
<td>Carrier Tracking</td>
<td>C.T.</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Gal/GPS</td>
<td>B/L</td>
<td>H/L</td>
<td>M/M</td>
</tr>
<tr>
<td>Hybrid PVT</td>
<td>C.T.</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Gal/GPS</td>
<td>L/L</td>
<td>L/L</td>
<td>-</td>
</tr>
<tr>
<td>Interference Mitig.</td>
<td>C.T.</td>
<td>no</td>
<td>no</td>
</tr>
<tr>
<td>Gal/GPS</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Multipath Mitig.</td>
<td>C.T.</td>
<td>no</td>
<td>no</td>
</tr>
<tr>
<td>Gal/GPS</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Measur.-quality Estim.</td>
<td>C.T.</td>
<td>no</td>
<td>no</td>
</tr>
<tr>
<td>Gal/GPS</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Advanced Positioning with</td>
<td>C.T.</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>limited signal</td>
<td>Gal/GPS</td>
<td>H/M</td>
<td>H/M</td>
</tr>
</tbody>
</table>
**GARDA Rx Prototype**

**Galileo System:**
- E5 (E5A and E5B)
  - $f_{RF} = 1176.45, 1207.14$ MHz
- E6 $f_{RF} = 1278.75$ MHz
- L1 $f_{RF} = 1575.42$ MHz

**GPS System:**
- L1 $f_{RF} = 1575.42$ MHz

**Signal Bandwidth**

<table>
<thead>
<tr>
<th>Signal Bandwidth</th>
<th>Galileo System:</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>E5 (E5A and E5B)</td>
</tr>
<tr>
<td></td>
<td>$f_{RF} = 1176.45, 1207.14$ MHz</td>
</tr>
<tr>
<td></td>
<td>E6 $f_{RF} = 1278.75$ MHz</td>
</tr>
<tr>
<td></td>
<td>L1 $f_{RF} = 1575.42$ MHz</td>
</tr>
</tbody>
</table>

**Number of Channels**

- Up to 16 configurable channels

**1 MFC**

- SFC0 (SFC L1)
- SFC1 (SFC E6)
- SFC2 (SFC E5A)
- SFC3 (SFC E5B)

**Sampling Freq**

- Baseline 95 MHz

**IF**

- Baseline 70 MHz

**A/D Converter**

- 3 Bit

**External Ref. Clock**

- 10 MHz
ANTENNA INTERFACES:

• 2 connectors providing L1 and E6+E5 signals

FRONT PANEL INTERFACES:

• 4 RF INPUT (L1, E6, E5a, E5b): SMA connectors to be connected to the Antenna (through the Power Splitter embedded in the chassis)

• CLOCK IN, CLOCK OUT: SMA to be connected to an external clock and distribute reference clock (from RF board master to slave)

• 4 IF analog OUT: to provide access to IF signals before AD conversion

• 1 RS232 Serial Data Communication I/F for PC data and command exchange

• 1 JTAG I/F for DSP up-loading

• 1 PPS and I/Q Signals Monitor
• Developed by SATIMO
• Wide Range to cover Galileo/GPS freq.
• Active, Triple frequency L1, E5, E6
• Double element structure (L1 and E5+E6)
• Pre-filtering (before the LNA) to avoid saturation and post filtering (after LNA) to improve out-of-band rejection

Example:
DUAL BAND STACKED CIRCULAR PATCHES
- 4 RF/IF (L1, E5a, E5b, E6) on two 3U boards
- Internal TCXO (10 MHz)
- Single-stage IF down-conversion targeted for low phase noise
- AGC/ADC on board
DSP Board

- Proprietary design, re-programmable computing platform for signal processing Galileo applications

- Based on the ADSP-21060 40MIPS SHARC® DSP Microcomputer and on the XILINX Virtex-II™ XC2V8000 FPGA.

- The DSP is able to sustain 80MFLOPS performances, while the Virtex-II™ has in charge to process up to four RF Complex Data Chains received from the Down Converter Board

- For testing purpose, 1Gbit DataFlash® Memory Card can be plugged on the module and read continuously in order to simulate one Galileo digital channel
**DSP Board**

- 4MB Flash Memory to store execution software
- 1.5MB 0 Wait-States SRAM to store PRN Codes
- 128KB of Boot Memory (on socket)
- 40Mhz Oscillator On Board
- 32MB Flash In-System Programmable Configuration PROM for FPGA programming
- High Speed LVDS Interface to acquire four Complex Digital Channels
- RS232 Interface PC Communication Channel
- JTAG Links to program both the FPGA and the DSP
- External Interface dedicated to the Pulse Per Second and Integration Epoch to synchronise optional Correlation Modules
- Double Serial Digital to Analog Converter to monitor the Complex Data Decoded
- External Command Interface through Serial Port to program the Down Converter Board
- Test Memory Plug In Interface to Down Load the Test Data Samples
FUNCTIONAL

- Input digitized samples @ Fs (3 bits)
- 4 input RF data streams: E5a, E5b, E6, L1
- Based on N (max 4) configurable SFC (data+pilot) for each MFC
- Measurements Epoch synchronous to all channels

PERFORMANCE

- Dynamic capability to support rural vehicle (vel < 100 m/s, acc < 10 m/s²) and aeronautical (vel < 128 m/s, acc < 20 m/s²)
- Carrier tracking 3rd order PLL with programmable BW
- Code tracking 2nd order DLL with programmable BW
- Carrier phase accuracy: 5 mm @ 35 dBHz
- Code phase accuracy: ranging from 20 cm to 50 cm @ 35 dBHz according to carrier & environment
- Tracking threshold: <= 30 dBHz according to carrier & environment
- Acquisition threshold: <= 35 dBHz according to carrier & environment
Proprietary Channel Design
FRONT-END
- Input digitized samples @ Fs (3bits)
- 4 input RF data streams: E5a, E5b, E6, L1
- AGC Level control
- Real To Complex Converter & FIR

CHANNEL MATRIX
- IF input MFC Multiplexer
- Single-Frequency Channels
  • Phase Rotator & Carrier Removal
  • Code Generator Unit
  • Code Delay Line & Correlation Unit

DSP/CPU INTERFACE
- Command/Data Registers interface
- Interrupt generation
- Link Port for FFT data downloading

TIME BASE GENERATOR
- Meas Epoch
- PPS
Channel development performed by Simulink-based (GRANADAR) bit-true design and performance simulation

- VHDL coding
- Test patterns generated by GRANADA and used to verify VHDL functions in ModelSim against Simulink design
- Test patterns generated by GRANADA and used to verify FPGA implementation using I/Q samples injected through DSP Test Memory
- Test patterns generated by GRANADA and used to verify FPGA using I/Q samples converted to RF through Rhode-Schwartz Vector Signal Generator

GARDA PROTOTYPE RECEIVER ARCHITECTURE
GARDA Receiver Testing

RECEIVER TESTS with DSP TEST MEMORY:

- Proto DSP board basic test:
  - Electrical and Functional Test

- VHDL integration
  - Test Memory loaded through PC-interface with I/Q samples generated by GRANADA
  - Test Memory Board communication to test basic functionality as:
    - registers interface
    - Interrupt controller
    - Correlation module
    - Observable measurements
RECEIVER TESTS with GALILEO Vector signal Generator:

RECEIVER TESTS with GPS Spirent Simulator STR4500:
RECEIVER TESTS with Proto GALILEO SPIRENT MCS TEST-BED:

- Signal & Noise Measurements
- Acquisition Performance
  - Time & Probability
  - Warm start
  - Cold start
- Tracking Thresholds Characterization
- Code/CARRIER Phase Noise
- Signal Tracking
- Dynamic Limits
- CPU Load
SIGNAL TO NOISE RATIO TEST

- Test aims to verify linearity of C/No measurement and to verify RRX implementation losses
- The simulator power output has been measured with a spectrum analyzer
- Verification of the simulator power control linearity
- Measurement of the receiver signal to noise ratio with assumption of thermal noise at the antenna input
- Verification of the receiver implementation loss taking into account the CASM modulation sharing losses
- 6.5dB have been considered for L1C power sharing losses
GARDA Test Results

Results

- C/No measurement is linear up to 45dBHz
- RRX average losses are less than 1.75 dB (including antenna front-end)
- The spectrum analyzer measurements is quite noisy
- Over 48 dBHz C/No estimator tends to saturate and this shows increase in RRX loss curve
PSEUDORANGE AND CARRIER THERMAL NOISE MEASUREMENTS

- Satellite signals cleaned of any simulated error (atmosphere or satellite clocks)
- Dynamic user: circular track scenario with \( v = 140 \text{m/s} \) and \( r = 1960 \text{m} \) to simulate wanted accel.
- Pseudorange noise computed by subtracting carrier measurement to remove satellite dynamic.
OBJECTIVE:
verify that the receiver acquired the signals
within a max given time in warm start condition

RESULTS:
L1C BOC(1,1) modulation
Two powers tested: 31dBHz and 33dBHz.
In the first case probabilities of acquisition were
of 65% while in the second case of 95%.
Average acquisition time around 20-25 seconds

Results match with theoretical
expectations with current setting
of acquisition parameters
“Bump and Jump” Technique on the stage between acquisition and tracking to remove false acquisition on side peaks. The receiver was set to search for the transmitted BOC(1,1) code on multiple channels. Cases were observed where one channel would acquire and track the main peak, while another channel would acquire and track the side peak. The channel tracking the main peak is at the expected power of 33 dB-Hz, while the channel tracking the side peak is at the expected side peak power 6 dB lower at 27 dB-Hz.

Probability that the Magnitude of one of the Secondary Peaks is Higher than the Magnitude of the Main Peak

SIDE PEAK FALSE ACQUISITION

NO ACQ
SIDE PEAK: 2.5% at 33 dB-Hz
GARDA Test Results

OBJECTIVE:
Verify tracking threshold lower limits

Test consisted in dropping quickly signal power down to 30dBHz, and from that point, further reducing power slowly (1dB / 30sec)

RESULTS:
an average loss of lock signal to noise ratio of 25.4 dBHz and a worst case loss of lock signal to noise ratio of 28.3 dBHz.
INTEGRATION & TEST PHASE

- Prototype HW-SW Integration completed for first BB model
- L1 Signal tests completed, E5 signal tests on-going, E6 scheduled
- Testing Phase currently running using GPS/GALILEO signals using SPIRENT Simulator. Live SV test performed for GPS; for GALILEO set-up ready for tracking GIOVE-A signal
- Optimum performance verified for all tested parameters (fully in line with requirements specification)

ACTIVITIES EXPECTED NEXT PERIOD

- Functional and Performance GALILEO Test using SPENG SIMULATOR (April-May 2006)
- Final Meeting: end of May 2006
- BB delivery: end of May 2006
Galileo Integrated Receiver for Advanced Safety of Life Equipments

- Project performed within the frame of GJU 2nd call (Receiver Technology)
- Two year project started September 2005

Objectives:
- Development of technologies and basic elements of a SoL Galileo Rx
- Develop a Rx prototype for Railway, Avionics, Maritime safety-critical applications in order to
  - Support standardization
  - Start Certification within each User Community
  - Facilitate market penetration of Galileo
- Make Rx prototypes available at early stage
- Develop a GALILEO Four Channel Signal Simulator
GIRASOLE Overview

- International Consortium lead by AAS-I

Manufacturers:
- design & development of SoL receivers breadboards
- core technologies identification and investigation

Scientific & Technical Team:
- provide scientific & technical support for core technologies identification and investigation
- provide support in the development of the identified core technologies
The SoL Receiver is a combined Galileo/EGNOS/GPS Receiver conceived to be used in the following applications:

- Aviation
- Maritime
- Rail

The receiver is possibly based on a common core and application specific parts.

The receiver processes Galileo signals on the L1, E5b bands and the GPS/EGNOS signals on the L1 band.

The receiver provides the following main functions:

- Combined Galileo+GPS Navigation solution
- Integrity calculations (HMI, Critical Satellites Prediction and Navigation Warning) using Galileo and EGNOS integrity message
- Interference and multipath mitigation
- Support the use of Local Elements
- Output raw measurements data for each satellite
GIRASOLE Receiver

Development Approach

1. INPUT to the Project (e.g. GARDA)
2. REQUIREMENTS and SPECIFICATIONS
3. CORE TECHNOLOGIES Investigation and Identification
4. TEST TOOLS and COMMON PLATFORM
5. BREADBOARD Development

COORDINATION with OTHER PROJECTS
The receiver architecture is based on a common core and some specific parts related to the application.

**Common core:**
- RF to IF down conversion,
- HW/ SW Signal Processing,
- Standard Navigation SW
- Integrity Processing

**Application specific:**
- Antenna
- RF Front End filtering
- Application dependant HW and SW (Interfaces)
## GARDA Re-use

<table>
<thead>
<tr>
<th>Receiver Element</th>
<th>Sub Element</th>
<th>Common Platform</th>
<th>GARDA Reuse</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Antenna System</td>
<td>Radiating Element</td>
<td>Dual narrow band (stacked patches)</td>
<td>YES</td>
<td>Common to all applications</td>
</tr>
<tr>
<td>LNA</td>
<td>Low noise figure</td>
<td>High gain, Low power consumption</td>
<td>YES</td>
<td>Common to all applications</td>
</tr>
<tr>
<td>RF Filters</td>
<td>E5b, L1 are the required signals</td>
<td>YES</td>
<td>Tailored to different interference environment. In particular, the Aviation application needs filter reassessment following the indications of the adopted standards</td>
<td></td>
</tr>
<tr>
<td>Mechanical aspects (box, shape, stiffness etc.)</td>
<td>GARDA breadboard is based on a 3U cPCI-like architecture that can be maintained.</td>
<td>YES</td>
<td>Specialised solutions may be required for different applications coping with different temperature limits. Mechanica stress can vary so much: customised solutions could be required. Different shapes</td>
<td></td>
</tr>
</tbody>
</table>
### GARDA Re-use

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<th>Common Platform</th>
<th>GARDA Reuse</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF / IF Section</td>
<td>Down Conversion scheme</td>
<td>Single stage analog downconversion</td>
<td>YES</td>
<td>IF Filter</td>
</tr>
<tr>
<td>ADC</td>
<td>3-bit ADC</td>
<td></td>
<td>YES</td>
<td></td>
</tr>
<tr>
<td>AGC</td>
<td>40 dB dynamic range compensation</td>
<td></td>
<td>YES</td>
<td></td>
</tr>
<tr>
<td>PLLs</td>
<td>Digitally Programmable PLLs</td>
<td></td>
<td>YES</td>
<td></td>
</tr>
<tr>
<td>IF Filter</td>
<td>70 MHz Intermediate Frequency Standard</td>
<td></td>
<td>YES</td>
<td>Following adopted frequency plan</td>
</tr>
<tr>
<td>Frequency Plan</td>
<td>Optimised to limit generated spurious and harmonics Carrier residual minimisation</td>
<td></td>
<td>YES</td>
<td>Customised frequency plan may be required by application dependent interference environment</td>
</tr>
</tbody>
</table>
## GARDA Re-use

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<th>Common Platform</th>
<th>GARDA Reuse</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSP Board</td>
<td>DSP Processor</td>
<td>The three different applications appear very similar in terms of required computing power, memory needs and processing speed. This encourages the development of a common processor board.</td>
<td>NO</td>
<td></td>
</tr>
<tr>
<td>Signal Processing</td>
<td>VHDL</td>
<td>Galileo digital channel behavioural model (one channel, all GALILEO frequencies)</td>
<td>YES</td>
<td>The minimum required number of multi-frequency channels is 4. The GARDA model must be up-graded</td>
</tr>
<tr>
<td>Integrity</td>
<td>Intergrity Algorithms</td>
<td>The management of the signal integrity is considered not application dependent. Consequently the development of the algorithms can be done as a common core. It is not part of the pre-existing GARDA software.</td>
<td>NO</td>
<td></td>
</tr>
</tbody>
</table>
Conclusions

- The Galileo Receiver is a challenging development due to new technologies, in particular for Signal Processing.
- GIRASOLE Project gives the opportunity to make receiver breadboards available for the User Community ready to support navigation applications as soon as the Galileo System is working.
- GARDA is the base point for the development providing a well proven set of tools and consolidated experience:
  - GRANADA SW Receiver Development Tool
  - Galileo Mono-Channel RF Simulator
  - Receiver Core technologies studies output
  - A Galileo Receiver Prototype