


A3SysDef: Aurora Avionics Architecture System Definition

(Contract ESTEC 17450/03/NL/LvH)

Final Report

October 14th, 2005

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A3SysDef (Aurora Avionics Architecture System Definition) is an ESA project (Contract ESTEC 17450/03/NL/LvH) conducted by a consortium led by EADS Astrium SAS with SciSys. For more information please contact:



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ESA STUDY CONTRACT REPORT			
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<p>ABSTRACT:</p> <p>The project objectives were to define an Aurora Avionics reference architecture, suitable to support different exploration missions, up to the generation of preliminary design specifications. This definition took into account the on-going development of HICDS by Laben SpA for Bepi Colombo.</p> <p>The project was split in two phases. The first phase investigated the lessons learnt from operational and planned exploratory missions, to write a set of system requirements about avionics (User Requirements and Implementation Constraints). The main outputs of this phase were the System Functional and Performance specification, and a model of the Avionics Functional Architecture. On the SW side, the application of SOIS to Aurora has been baselined, and a set of three services has been analysed and modelled. The second phase focused on the definition of a toolbox, providing early definition of components (ASICs), modules and equipments. Trade-offs have been performed and preferred candidates for architecture and implementation have been selected. Detailed design specifications have been issued for the Solid State Mass Memory, the Payload Unit, the GNC/AOCS Support Unit and the μRemote Terminal Unit; and on Basic and Standard Services for the SW. A technology road-map and development plan, and an application analysis for the ExoMARS and MSR missions, have been issued.</p>			

Deliverables Phase 1:

- TN 1.1 FPR “Function and Performance Requirements for interplanetary missions”
- TN 1.2 AIC “Avionics Implementation Constraints”
- TN 1.3 URD “User Requirements Document”
- TN 1.4 SFP “System Functional and Performance Requirements”
- TN 1.4 RDP “Aurora preliminary Roadmap and Development Plan”
- TN 1.4 FSM “Formal Specification Model”
- TN 1.5 AFA “Avionics Functional Architecture”
- TN 1.6 TN2 “Applying CCSDS-SOIS to the Aurora Avionics Architecture”

Deliverables Phase 2:

- TN 2.1 AAI “Design Report of the Avionics Architecture Implementation” (includes TN 2.7 FSM)
- TN 2.1 EAA “Engineering trade-offs assessments and analysis”
- TN2.1.a EAA “Aurora Basic Software & Standard Services Users Requirement Document”
- TN 2.2 ATS “Avionics Toolbox Specification”
- TN 2.4a DS-MMSD “Design Specification: Mass Memory Storage Device”
- TN 2.4b DS-PPPM “Design Specification: Payload Peripheral Processing Module”
- TN 2.4c DS-SSSF “Design Specification: Support to System Specific function”
- TN 2.5 PIL/SCS “Platform Interconnection Layout Rules + Support Component Specification”
- TN 2.6 DS-BSSS “Design Specification: Basic Software and Standard Services”
- TN 2.6 FSW “UML model of the SW design”
- TN 2.7 FSM “Formal Specification Model update” (included in TN 2.1 AAI)
- TN 2.8 RDP “Aurora Technology Roadmap and Development plan” (updated from Phase 1)
- TN 2.9 FR “Final Report” (the present document)
- TN 2.10 TN2 “Applying CCSDS-SOIS to the Aurora Avionics Architecture” (updated from Phase 1)
- Final presentation slides

The work described in this report was done under ESA contract. Responsibility for the contents resides in the author or organisation that prepared it.

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1 Introduction

1.1 Scope

1.1.1 Scope of the Project

A3SysDef (Aurora Avionics Architecture System Definition) is an ESA project (contract ESTEC 17450/03/NL/LvH). The project objectives were to define an Aurora Avionics reference architecture, suitable to support different exploration missions, up to the generation of preliminary design specifications. This definition took into account the on-going development of HICDS by Laben SpA for Bepi Colombo.

The project was split in two phases:

The first phase investigated the lessons learnt from operational and planned exploratory missions, to write a set of system requirements about avionics (User Requirements and Implementation Constraints). The main outputs of this phase were the System Functional and Performance specification, and a model of the Avionics Functional Architecture. On the SW side, the application of SOIS to Aurora has been baselined, and a set of three services has been analysed and modelled.

The second phase focused on the definition of a toolbox, providing early definition of components (such as ASICs), modules and equipments. Trade-offs have been performed and preferred candidates for architecture and implementation have been selected. Detailed design specifications have been issued for the Solid State Mass Memory, the Payload Unit, the GNC/AOCS Support Unit and the μ Remote Terminal Unit; and on Basic and Standard Services for the SW. A technology road-map and development plan, and an application analysis for the ExoMARS and MSR missions, have been issued.

1.1.2 Scope of the Document

This document is the Final Report of the A3SysDef project. It covers the whole project (phase 1 and phase 2) and gives an overview of the project organisation, structure and main findings, outcomes and recommendations.

This introduction provides:

- The scope of the project and of this document (this section),
- The list of related documentation (A3SysDef reference and applicable documents, list of A3SysDef management documents, and A3SysDef technical documents and delivered products),
- The terminology and acronyms used in this document.

After this introduction, this Final Report is split in 2 chapters.

Chapter 2 describes the A3SysDef project from an organisational viewpoint:

- Objectives of the project,
- Consortium information,
- Study Logic,
- Project Outputs: technical notes, software products, models and presentations.

Chapter 3 describes the project from a technical viewpoint, providing a synthesis of the activities, rationale and main findings and results of each one of the project tasks. The chapter 3 concludes with a section providing a synthetic summary of the main project results and recommendations.

1.2 Related Documentation and Products

1.2.1 *Applicable Documents*

- [FPR] Functional and performance requirements for ESA planetary missions
EAA.NA.87703.ASTR, issue 1, 16/12/2003
- [AIC] Avionics Implementation Constraints
EAA.NA.87704.ASTR, issue 1, 30/01/2004
- [URD] User requirements document
EAA.SP.87705.ASTR, issue 1, 16/12/2003
- [SFP] System Functional and Performance specification
EAA.SP.87706.ASTR, issue 1, 04/02/2004
- [SOW] Statement of work Aurora Avionics Architecture System Definition
Esd/pp/674.02, issue 1, 30/09/2002
- [SOW-AD1] Packet Telecommand Standard PSS-4-107 Issue 2, April 1992, ESA
- [SOW-AD2] Packet Telemetry Standards PSS-4-106 Issue 1, January 1988, ESA
- [SOW-AD3] Mil-STD-1553-B Notice 2 Digital Time Division Command/Response Multiplex Data Bus
- [SOW-AD4] Spacecraft Data Handling Interface Standards
- [SOW-AD5] PCI Local Bus specification
- [SOW-AD6] Compact PCI Specifications PICMG 2.0, R2.1 2 September 1997
- [SOW-AD7] CAN Specification Version 2.0 - BOSCH
- [SOW-AD8] I2C Specifications - Philips Semiconductor
- [SOW-AD9] IEEE Standard for a High Performance Serial BUS IEEE Std 1394-1995
- [SOW-AD10] AMBA bus specification
- [SOW-AD11] European Cooperation for Space Standardisation (ECSS). Space Engineering. Software – Space Segment. ECSS-E-40-01 Issue 1 October 2000
- [SOW-AD12] ASIC Design and Manufacturing Requirements, WDN/PS/700 Issue 2, October 1994, ESA.
- [SOW-AD13] VHDL Modelling Guidelines, ASIC/001 Issue 1, September 1994
- [SOW-AD14] Telecommand Decoder Specification, ESA PSS-04-151 Issue 1, September 1993
- [SOW-AD15] Telemetry Channel Coding Standard, ESA PSS-04-103, Issue 1, September 1989
- [SOW-AD16] Telemetry Channel Coding CCSDS 101.0-B-4, Blue Book, Issue 4, May 1999
- [SOW-AD17] Packet Telemetry, CCSDS 102.0-B-4, Blue Book, Issue 4, November 1995

- [SOW-AD18] Telecommand Part 1 -- Channel Service, CCSDS 201.0-B-3, Blue Book, Issue 3, June 2000
- [SOW-AD19] Telecommand Part 2 -- Data Routing Service, CCSDS 202.0-B-2, Blue Book, Issue 2 November 1992
- [SOW-AD20] Telecommand Part 2.1 -- Command Operation Procedures, CCSDS 202.1-B-1, Blue Book. Issue 1 October 1991. (TBC)
- [SOW-AD21] Telecommand Part 3 -- Data Management Service, CCSDS 203.0-B-1, Blue Book. Issue 1 January 1987. (TBC)
- [SPW] SpaceWire – Links, nodes, routers and networks, ECSS-E-50-12A, 24 January 2003

1.2.2 Reference documents

- [SOW-RD1] Technologies for exploration - Aurora Programme Proposal: Annex D - ESA SP-1254
- [SOW-RD2] ftp://ftp.estec.esa.nl/pub/aurora/ESA-HQ_16-17_07_2002/
- [SOW-RD3] An Highly Integrated Control and Data System in support of a Planetary Observer mission' Patrick Plancke DASIA 2002 Dublin ESA SP 509
- [SOW-RD4] CCSDS 'S/C On board InterFace '
- [SOW-RD5] Satellites, Data System Standards Application Layer for Data Handling Interfaces (DH) On-Board Spacecraft ETSI/DEN/SES-001-ECSS2-2
- [SOW-RD6] HICDS SOW
- [SOW-RD7] MIAE SOW
- [SOW-RD8] CCSDS Sensor bus workshop proceedings - Austin October 2002
- [SOW-RD9] OAR. RTEMS SPARC Application Supplement
- [SOW-RD10] Open Ravenscar Kernel Technical University of Madrid
- [SOW-RD11] The Ravenscar profile, Burns A, Ada letters,XIX (4), ACM Press (1999) 49-52
- [SOW-RD12] Packet Utilisation Standard
- [SOW-RD13] CFDP (CCSDS File Distribution Protocols) CCSDS Blue Book
- [HICDS-01] HICDS System Requirements, P-HICDS-SPC-00001-SE, issue 7, 31/3/2002
- [HICDS-02] HICDS core hardware ICD, TL 18995, issue 3, March 2003
- [HICDS-03] SCTMTC ASIC User's Manual, P-ASIC-NOT-00122-SE, issue 4, 26/02/2003
- [HICDS-04] HICDS Synthesis, TL 20224, issue 1, 14/11/2003
- [HICDS-05] Astrium requirements assessment, TL 20457, 20/02/2004
- [HICDS-06] HICDS Evolution, implementation trade-offs and top level avionics architecture, TL 21044, 18/11/2004 (+ EADS-Astrium comments on this document and their answers by Laben within ML. Esposti e-mail 09/02/2005)
- [EXM-01] CDF Study Report ExoMars09, CDF-14(A), August 2002

- [EXM-02] ExoMars phase A SOW, Aurora/001.03, issue 1 rev 3, 11/04/2003
- [EXM-03] TN4 – ExoMars Rover/Pasteur : System & Subsystem Design Report, ROV.TN.04.EU.ASTR
- [EXM-04] EXOMARS Orbiter / Carrier Design Report, EXO-TN-ASF-017 issue 2, 09/07/2004
- [MPR-01] Proposition Mars Premier Orbiteur MO'07, Dossier de Définition & Justification orbiteur, orbiter design (chap. 4) and equipment design (chap. 7)
- [MSR-01] MSR Study overview, final presentation slides, 18/02/2003
- [MSR-02] Mars Sample Return SOW, AURORA/AS/kc/002.03, issue 2, 12/05/2003
- [ERV-01] Pre-Phase 1 Study of Earth Re-entry Vehicle / Capsule SOW AURORA/003.03, issue 1 rev 5, 27/02/2003
- [ASW-01] Aurora Basic Software and Standard Services User Requirements (SW-URD), AOE7.URD.92854.ASTR, issue 2, 03/02/2005
- [ASW-02] Basic Software and Standard Services Design Specification SSL/D7929/DOC/0001, issue 1 rev 1, 20/05/2005

1.2.3 A3SysDef delivered management items

- [ABS] A3SysDef Abstract, June 30, 2005.
- [FR] A3SysDef Final Report, September 8, 2005 (this document).
- [MM1] A3SysDef Minutes of meeting: AOE7.MIN.90275.ASTR 28-6-2004
- [MPR1..8] A3SysDef Monthly Progress Reports 1 to 8.

1.2.4 A3SysDef delivered technical items for Phase 1

- [PM1] A3SysDef PM1 and User Requirement Review 4/5-12-2003
- [PM2] A3SysDef PM2 and System Requirement Review 24/25-02-2004
- [MP] A3SysDef Mid-Term Presentation 10-03-2004
- [SOIS1] SOIS Working Meeting 07-06-2004
- [SOIS2] Avionics Architecture and SOIS Working Meeting 28-06-2004
- [A3SysDef PS1] Presentation Slides of the A3SysDef Final Phase 1 Presentation, ESTEC, Noordwijk, March 10, 2004
- [FPR] “Function and performance requirements for ESA planetary missions”, EADS-Astrium, EAA.NA.87703.ASTR, issue 1.0, December 16, 2003.
- [AIC] “Avionics implementation constraints”, EADS-Astrium, EAA.NA.87704.ASTR, issue 1.0, February 26, 2004.
- [URD] “System level User Requirement Document”, EADS-Astrium, EAA.SP.87705.ASTR, issue 1.0, December 20, 2003.
- [SFP] “System functional and performance specification”, EADS-Astrium, EAA.SP.87706.ASTR, issue 1.0, February 26, 2004.

- [RDP] “Aurora preliminary technology roadmap and development plan”, EADS-Astrium, EAA.PLD.87707.ASTR, issue 1.0, February 26, 2004.
- [AFA] “Avionics functional architecture”, EADS-Astrium, EAA.ADD.97709.ASTR, issue 1.0, March 05, 2004.
- [TN2] “Aurora Avionics TN2, Impact of CCSDS SOIS on Aurora Avionics”, S. Parkes (consultant), TN2, issue 1.0, April 28, 2004.

1.2.5 A3SysDef delivered technical items for Phase 2

- [PM3] A3SysDef Design specification and SW SRR meeting 21/22-04-2005
- [A3SysDef PS2] Presentation Slides of the A3SysDef Final Presentation, ESTEC, Noordwijk, September 8, 2005.
- [SW-URD] Aurora Basic Software & Standard Services Users Requirement Document, EADS-Astrium, AOE7.URD.92854.ASTR, issue 2.0, March 02, 2005
- [AAI] “Design report of the Avionics Architecture Implementation”, EADS-Astrium, EAA.DDD.89243.ASTR, issue 1.0, June 30, 2005. It includes the print of the Formal Specification Model update (FSM from WP 2.7)
- [EAA-1] “Communication Links Trade-Off, Engineering Trade-Off assessments and analysis”, EADS-Astrium, R&D.Aurora.NT.00350.V.ASTR, issue 1.0, May 27, 2005.
- [EAA-2] “I/O Architecture Implementation Trade-off, Engineering Trade-Off assessments and analysis”, EADS-Astrium, R&D.Aurora.NT.00351.V.ASTR, issue 1.0, May 27, 2005.
- [EAA-3] “SSMM Detailed Implementation Trade-off, Engineering Trade-Off assessments and analysis”, EADS-Astrium, R&D.Aurora.NT.00352.V.ASTR, issue 1.0, May 27, 2005.
- [EAA-4] “ μ RTU Architecture and Implementation Trade-off”, EADS-Astrium, R&D.Aurora.NT.00353.ASTR, issue 1.0, May 27, 2005.
- [EAA-5] “Power Supply Implementation Trade-Off, Engineering Trade-Off assessments and analysis”, EADS-Astrium, R&D.Aurora.NT.00354.V.ASTR, issue 1.0, May 27, 2005.
- [EAA-6] “Mechanical / Thermal Architecture Implementation Trade-Off, Engineering Trade-Off assessments and analysis”, EADS-Astrium, R&D.Aurora.NT.00355.V.ASTR, issue 1.0, May 27, 2005.
- [EAA-7] “PSU Architecture and Implementation Trade-Off, Engineering Trade-Off assessments and analysis”, EADS-Astrium, R&D.Aurora.NT.00356.V.ASTR, issue 1.0, May 27, 2005.
- [ATS] “Avionics Tool Box Specification”, EADS-Astrium, R&D.Aurora.NT.00363.V.ASTR, issue 1.0, May 27, 2005 completed by

	“Avionics Interface Control Document” R&D.Aurora.NT.00370.V.ASTR, issue 1.0, May 27, 2005
[DS-MMSD]	“Solid State Mass Memory Specification”, EADS-Astrium, R&D.Aurora.SP.00366.V.ASTR, issue 1.0, May 27, 2005.
[DS-PPPM]	“Payload Peripheral Processing Module Specification”, EADS-Astrium, R&D.Aurora.SP.00368.V.ASTR, issue 1.0, May 27, 2005 (aka PSU specification)
[DS-SSSF]	“GSU Specification”, EADS-Astrium, R&D.Aurora.SP.00367.V.ASTR issue 1.0, May 27, 2005
[DS-μRTU]	“μRTU Specification”, EADS-Astrium, R&D.Aurora.SP.00369.V.ASTR issue 1.0, May 27, 2005
[PIL/SCS]	“Platform Interconnection Layout rules”, EADS-Astrium, xxxx.ASTR, issue 1.0, July 13, 2005, including Support Component Specification.
[DS-BSSS]	“Basic SW and Standard Services Design Specification”, SciSys, SSL/D7929/DOC/0001, issue 1.1, May 20, 2005.
[FSW]	“UML model of the Software design”, SciSys, computer file A3SysDef_BasicSoftware v1.1.zuml
[FSM]	“Formal Specification Model update”, EADS-Astrium, computer file Aurora_Architecture.zuml.
[RDP]	“Aurora Technology Roadmap and Development Plan”, EADS-Astrium, R&D.Aurora.NT.xxx.V.ASTR, issue 1.0, July 05, 2005.
[FR]	“Final Report”, EADS-Astrium, A0E7.TCN.xxxxx.ASTR, issue 1.0, July 13, 2005 (the present document)
[TN2]	“Aurora Avionics TN2, Impact of CCSDS SOIS on Aurora Avionics”, S. Parkes (consultant), TN2, issue 2.0, August 28, 2005.

1.3 Acronyms and Abbreviations

AD : Applicable Document

AOCS : Attitude and Orbit Control System

CCSDS : Consultative Committee for Space Data Systems

EOL : End of life

GNC : Guidance Navigation Control

GSU : GNS/AOCS Support Unit

I/O : Input/Output

PSU : P/L Support Unit

RTU : Remote Terminal Unit

SCC Spacecraft Controller Core

SpW : SpaceWire

SSMM : Solid State Mass Memory

TBC : To Be Confirmed

TBD : To Be Defined

2 Project Organisation

2.1 Consortium

The A3SysDef project was performed by a consortium led by EADS-Astrium SAS (called Astrium SAS when the project started) with SciSys and the consultant S. Parkes.

The consortium relied on the EADS-Astrium knowledge and experience in space systems and space units development, complemented by SciSys and S. Parkes skills in advanced software technologies for embedded systems.

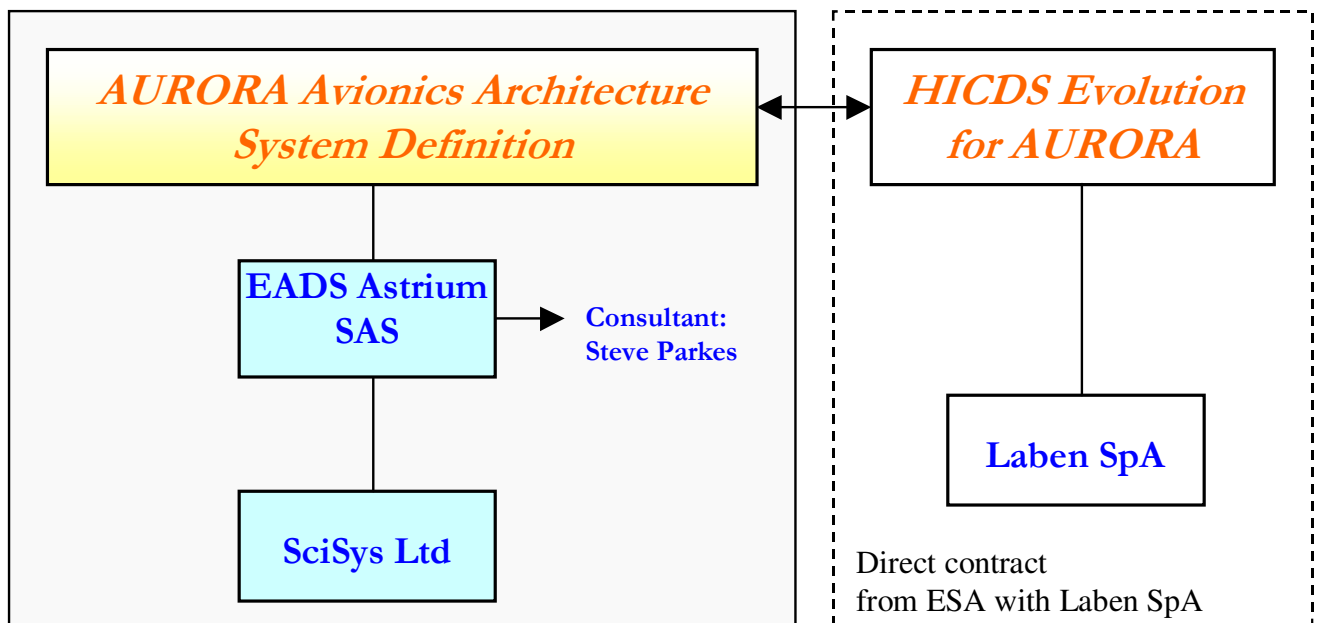


Figure 1 — A3SysDef industrial team and interfaces

People involved in A3SysDef Project:

ESTEC: Patrick Plancke (Technical Officer); Linda van Hilten (Contract Officer)

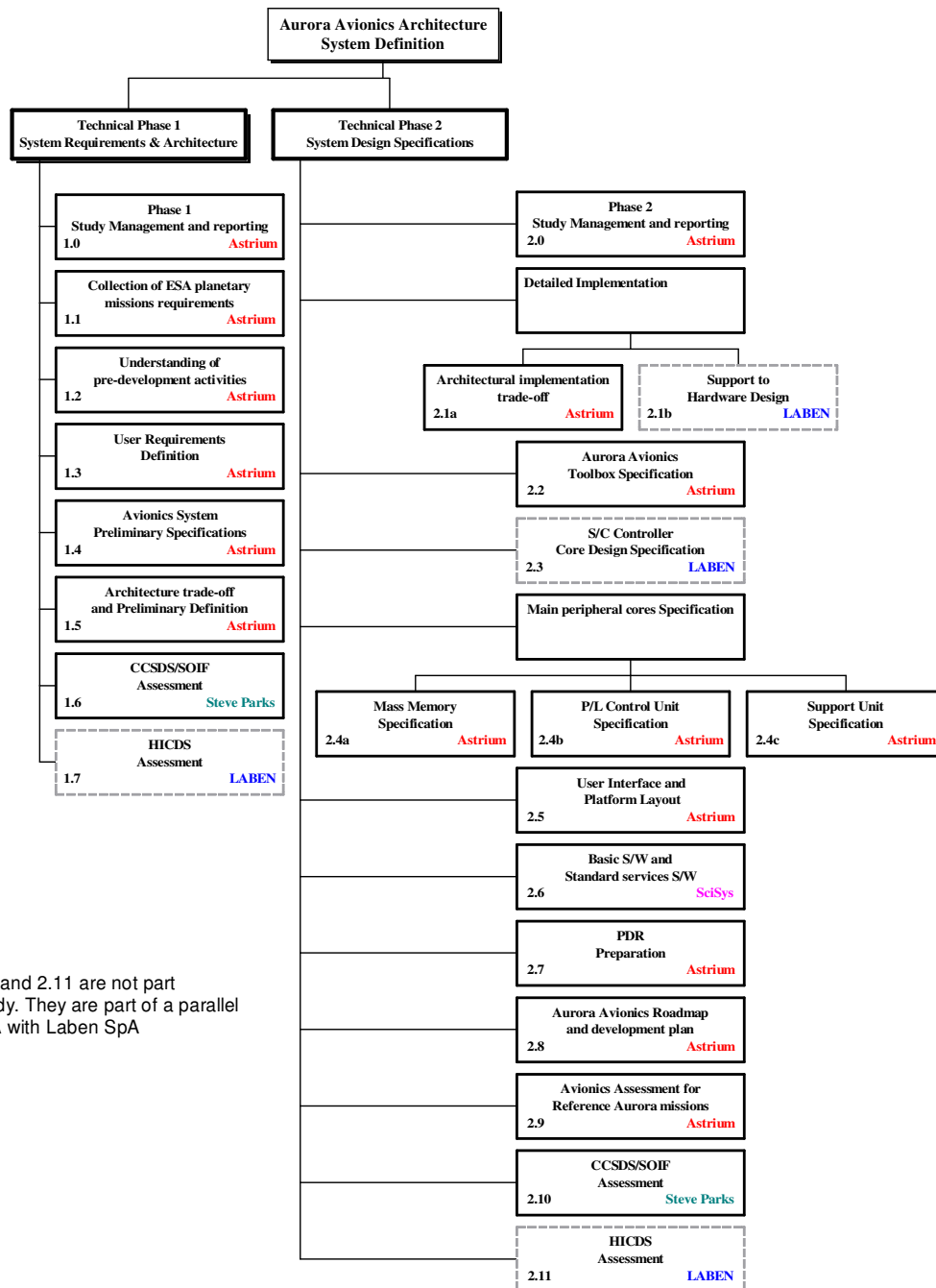
EADS-Astrium: Marc Le Roy replaced by Thierry Planche on April 2005 (Project Manager), Jacques de Urtasun (Contract Responsible) with Eric Maliet, Charles Koeck, Jean-François Coldefy, Philippe Jegoux, Gérard Nadalin, Laurent Soubrier, Luc Planche, Olivier Notebaert, Claude Carron, Nicolas Neugnot.

SciSys: Stuart Fowell (Responsible)

Steve Parkes (Consultant)

2.2 Study Logic

The A3SysDef project was split in two phases dedicated respectively to the definition of the Avionics User Requirements / Performances, and to the definition of a ToolBox and Unit Design Specifications (including SW detailed design and modelling). The technology road-map is a significant output of the project.



WP 1.7, 2.1b, 2.3 and 2.11 are not part of the present study. They are part of a parallel contract from ESA with Laben SpA

Figure 1 — A3SysDef Study Logic (phases 1 & 2)

Phase 1 covers the preliminary definition of the avionic architecture system, which has been presented at the end of this phase at the study's mid-term meeting. It embraced the following technical work packages:

- (WP1.1) Perform an analysis of Aurora early planetary missions in order to identify the driving functions and performance required for achieving them.
- (WP1.2) Identify the existing elements that can be usable as building blocks for the avionics architecture definition in understanding the pre-development activities.
- (WP1.3) Establish a user requirements specification that will drive the architecture definition.
- (WP1.4) Establish the specification of the required functions as well as the preliminary definition of the associated performances in response to the user requirements. The textual specification is written in parallel to a formal specification model.
- (WP1.5) Perform an architectural trade-off in order to define a preliminary avionics system architecture layout.
- (WP1.6) CCSDS and SOIF expertise and technical assessment.

In addition, the task (WP1.7) "HICDS assessment" has been done in the frame of the parallel study "HICDS Evolution for AURORA"

Phase 2 is dedicated to the avionics architecture detailed implementation trade-off up to a consolidated avionics architecture data package including HW and SW allocation, preliminary budgets (mass, power) and physical characteristics of the avionics nodes and inter-connections. At the end of the phase, a technological road-map is elaborated, and a preliminary design review is performed.

- (WP2.1a) Perform an implementation trade-off of the functional architecture defined during phase 1. Issue an Avionics Architecture Document which includes hardware architecture, software user requirements and preliminary software architecture. Provide technological data for mass memory and support unit HW modules of the avionics system including features and technical data assessment for the components performances. Assess feasibility of the avionics system architecture implementation trade-off through preliminary analysis on the physical data for these elements (mechanical, thermal, radiation...).
- (WP2.1b) in the frame of the parallel study "HICDS Evolution for AURORA", provide technological data expertise for HW modules of the avionics system including features and technical data assessment for the Spacecraft Controller Core and P/L extension. Support and assess feasibility of the avionics system architecture implementation trade-off through preliminary analysis on the physical data for these elements (mechanical, thermal, radiation...).
- (WP2.2) Identify the layers and building blocks of the avionics architecture – nodes and inter-connections. An interconnection toolbox is specified for characterization of each layer standards and interface. This aims at allowing a modular avionics platform which is able to support a large scope of missions and to allow local redesign for evolution in future technology implementation. A HW-HW and HW-SW ICD completes this WP.

(WP2.3) Out of the scope of the present study, but in the frame of the parallel study “**HICDS Evolution for AURORA**”, establishment of the Spacecraft Core Controller Computer design specifications (TM, TC, CPU, I/O, Reconfiguration, time management)

(WP2.4x) Establishment of the Main Peripheral Core design specifications:

(WP2.4a) Modular Mass Memory (SSMM)

(WP2.4b) Payload Peripheral Processor (PSU)

(WP2.4c) Specific Support System (GSU)

A μ RTU specification completes this WP 2.4. The HW-HW and HW-SW ICD from WP 2.2 is also relevant to this section.

(WP2.5) Definition of some interconnection layout rules allowing for mass and power consumption reduction. Specification of the corresponding Standard Support user interfaces components.

(WP2.6) Specification and analysis of basic software requirements.

(WP2.7) Update of the formal model of the Avionics architecture.

(WP2.8) Production of a road map and a development plan for completion of the Aurora avionics core elements and integration (H/W-H/W, H/W-S/W, S/W-S/W), including the development of ASIC(s) and modules and their qualification.

(WP2.9) Production of the study final report summarizing the achievements of the study and final presentation.

(WP2.10) CCSDS and SOIF expertise and technical assessment (update of TN2 from phase 1).

In addition, the task **(WP2.11)** “HICDS open architecture assessment” is done **in the frame of the parallel study “HICDS Evolution for AURORA”**.

The execution of the tasks during both phases has been supported by the following management and coordination work packages:

(WP1.0) Phase I study management and reporting.

(WP2.0) Phase II study management and reporting.

2.3 Project Outputs

The project technical outputs are presented by categories in the following sections and tables.

2.3.1 Issued documents

For Phase 1:

[FPR]	“Function and performance requirements for ESA planetary missions”, EADS-Astrium, EAA.NA.87703.ASTR, issue 1.0, December 16, 2003.
[AIC]	“Avionics implementation constraints”, EADS-Astrium, EAA.NA.87704.ASTR, issue 1.0, February 26, 2004.
[URD]	“System level User Requirement Document”, EADS-Astrium, EAA.SP.87705.ASTR, issue 1.0, December 20, 2003.
[SFP]	“System functional and performance specification”, EADS-Astrium, EAA.SP.87706.ASTR, issue 1.0, February 26, 2004.
[RDP]	“Aurora preliminary technology roadmap and development plan”, EADS-Astrium, EAA.PLD.87707.ASTR, issue 1.0, February 26, 2004.
[AFA]	“Avionics functional architecture”, EADS-Astrium, EAA.ADD.97709.ASTR, issue 1.0, March 05, 2004.
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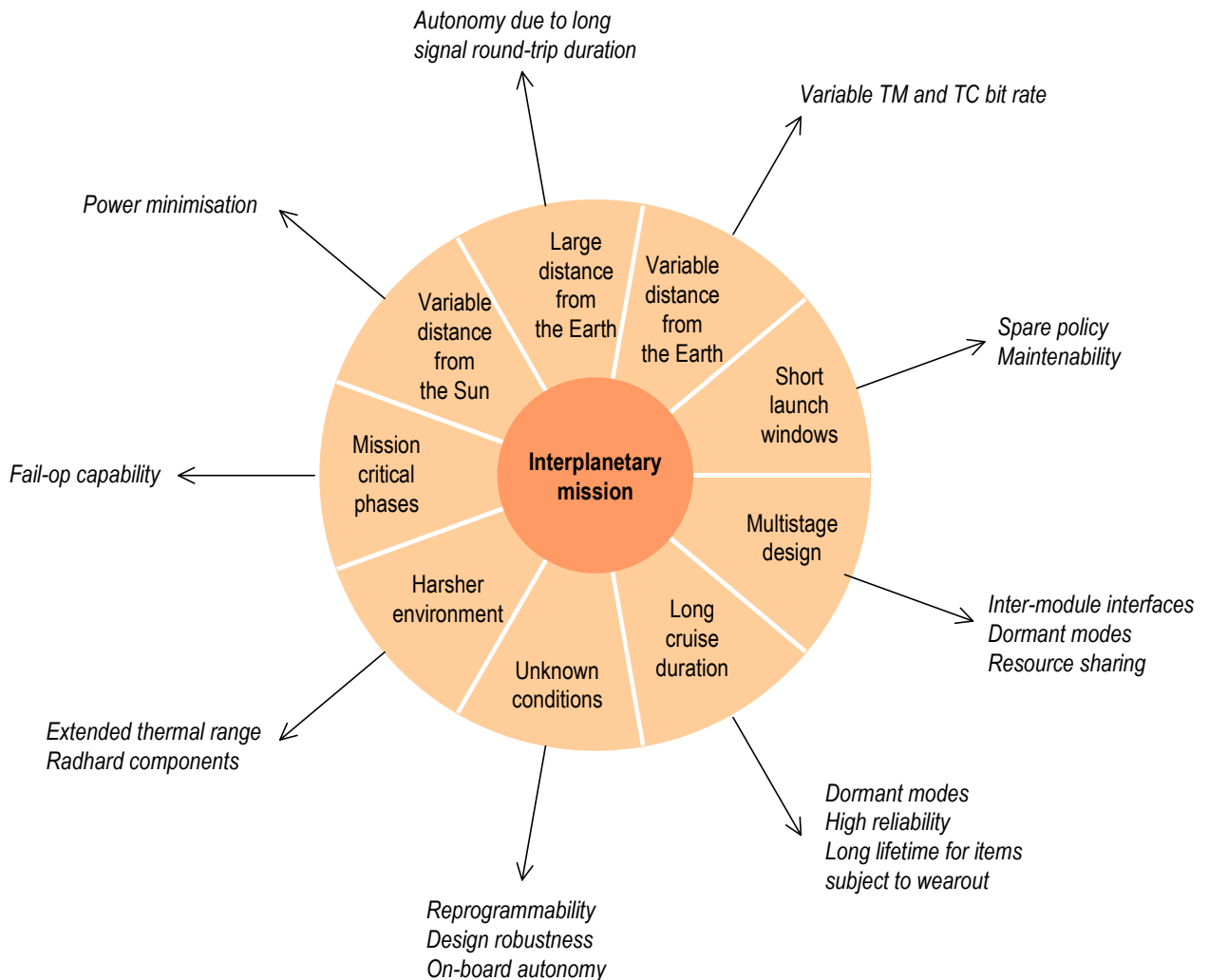
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- [EAA-4] “ μ RTU Architecture and Implementation Trade-off”, EADS-Astrium, R&D.Aurora.NT.00353.ASTR, issue 1.0, May 27, 2005.
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3 Synthesis of results

3.1 User requirements for planetary missions

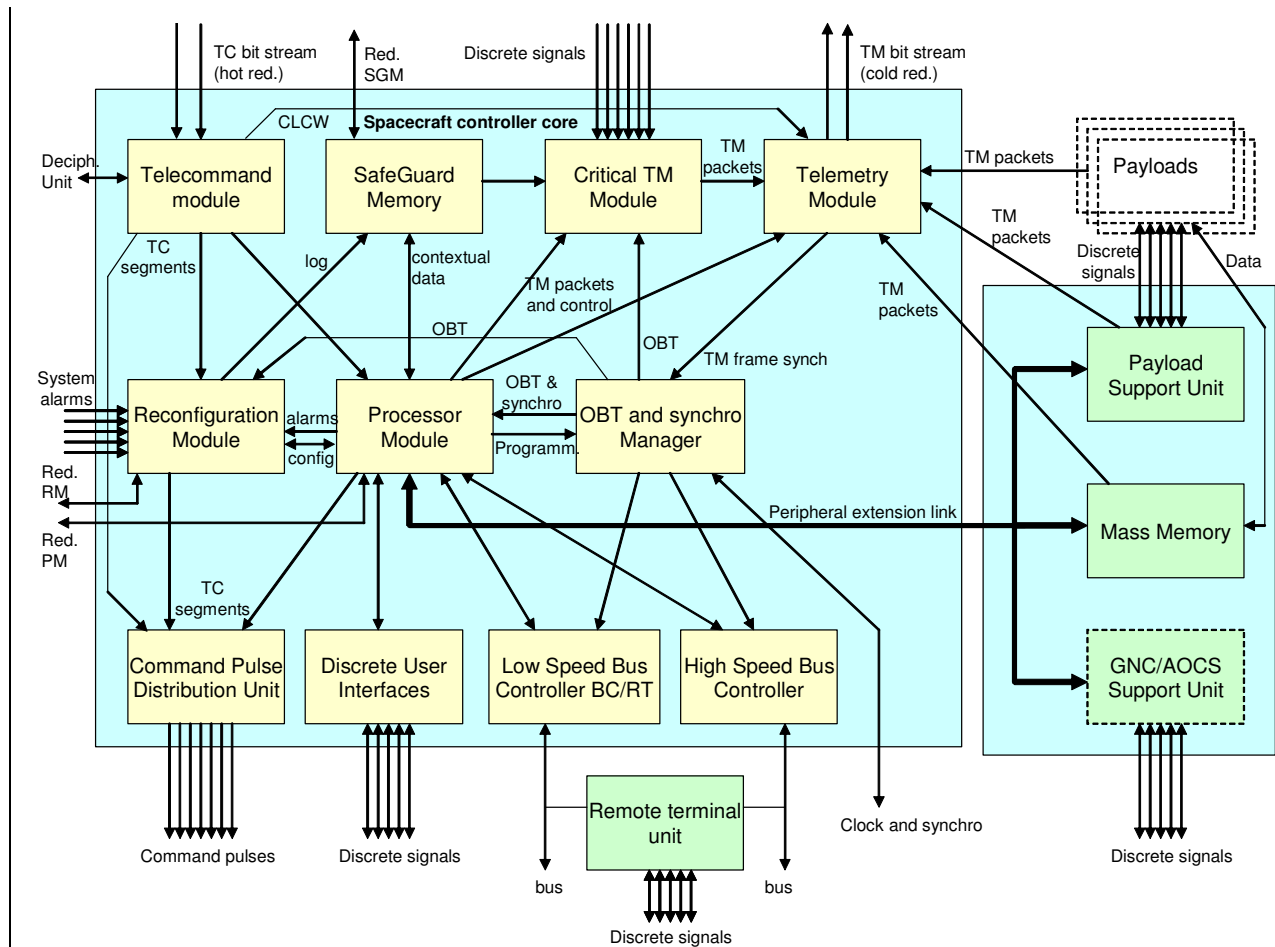
Past, present and future ESA planetary missions (including the on-going Aurora studies) are analysed to extract the functional & performance requirements. Focus is put on autonomy and environmental conditions, which are considered to be major design drivers for those missions.



The missions which has been studied include Rosetta, Mars Express, Venus Express, Bepi Colombo, Jupiter Microsat Orbiters, ExoMARS, Mars Sample Return, Earth Reentry Vehicle Demonstrator, Mars Aerocapture demonstrator, Crewed missions. Three families of interplanetary vehicles are identified: orbiters, landers (including rovers), launchers (including MSR Mars Ascent Vehicle or Mars take-off stage for a possible crewed mission).

3.2 Functional architecture

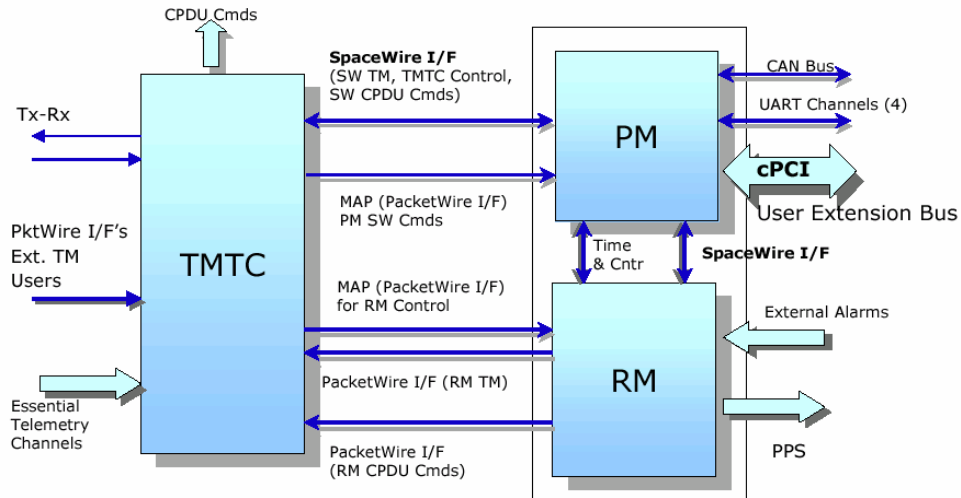
AURORA platform functional architecture is presented here below:



The implementation of this architecture for AURORA is mainly led by:

- The 3 different applications Orbiter, Lander or Launcher leading to be efficient for the modularity and scalability implementation of the different functional blocks.
- FDIR, Reliability, Autonomy and Availability that are also drivers for the modularity and the communication links.
- The power distribution that must be scalable for the different architectures with a minimum penalty from the simplest implementation to the biggest one.
- The Processing needs and the Overall software (BSP, MiddleWare, Applications) modularity for the various applications and various functional phases within the applications.
- The Environmental conditions of the missions (radiations, mechanical, thermal).
- The validation process for the various applications from the design to the qualification.
- A final system cost as low as possible.

The ESA request to use HICDS developed in another ESA contract framework. HICDS architecture is shown on figure hereafter:



- HICDS offers CAN bus interface, 4 x UART channels and proposes extensions through cPCI backplane bus. Unfortunately, HICDS offers neither user free SpaceWire links nor 1553 bus.
- The Processor Module (PM) is based on the LEON2-FT core. The PM communicates by SpaceWire links with the SCTMTC and the RM and by PacketWire for MAP of the SCTMTC. It provides a cPCI backplane bus, the CAN and UART interfaces.
- The TMTc Telemetry and Telecommand Module are based on the new SCTMTC ASIC developed by SES. The TM virtual channels can be connected to up to 8 x PacketWire links. The TC provides up to 64 x multiplexed MAP.
- The Module (RM) executes autonomous reconfiguration sequences. It includes a SafeGuard Memory (SGM). The RM communicates by PacketWire links with the SCTMTC and by a SpaceWire link with the PM.

3.3 Engineering trade-offs

Several trade-off as communication links, μ RTU architecture, SSR architecture, PSU architecture, Analogue I/O definitions, Power supplies solutions, Packaging solutions were necessary to find out one or more implementation solutions.

3.3.1 Communication links

The links inside AURORA architecture are between HICDS core, μ RTU, P/L & PSU, GSU, SSR and direct links with some peripherals as shown here before. The trade-off analyses different links based on redundancy, power consumption, implementation complexity, reliability and FDIR management (refer RD xx).

Communications are based on low speed (some hundred KHz or some MHz) bus for command/control and on point to point high-speed (some hundred of MHz or some GHz) link for data exchanges. In the future, there will be only high speed link (low speed link will be embedded in high speed links). This evolution has too many consequences (architecture, protocole, overall real-time performances) to be mature for AURORA.

Low speed bus can be based on CAN or 1553 bus types. Within a system only one bus type shall be implemented.

- 1553 MIL bus shall be upgraded to reach from 2 to 10 Mbits/s instead of 1 Mbit/s in accordance with new EEE standards. Both 1 Mbits/s and new higher speed can coexist to reuse current peripherals. 1553 is targeted for rather large systems thanks to EMC isolation properties of the electrical architecture.
- CAN could also be upgraded but is convenient as is, because mainly targeted to small to medium systems which do not mandatory need EMC isolation properties.

High-speed bus can be based on the SpaceWire (some hundred of Mbit/s) in order to take the benefit of on-going studies. Gigalink (1 or 2 Gbit/s) or PCI express (some Gbit/s to ten of Gbit/s) are future good candidates to interconnect modules inside units and between units. PCI express will be better because it is a commercial standard with development tools.

- Current SpaceWire SpW332 (3 nodes), SpW116 (1 node) and the router (8 nodes) parts will cover high-speed links architecture. Nevertheless, to ease the implementation in a heterogeneous system with numerous nodes, a low power generation should be studied to reduce power consumption when there is no traffic. It is also quasi mandatory to simplify the harness and the system qualification to study a router located in each unit instead of a centralised one.

As a result of AURORA studies:

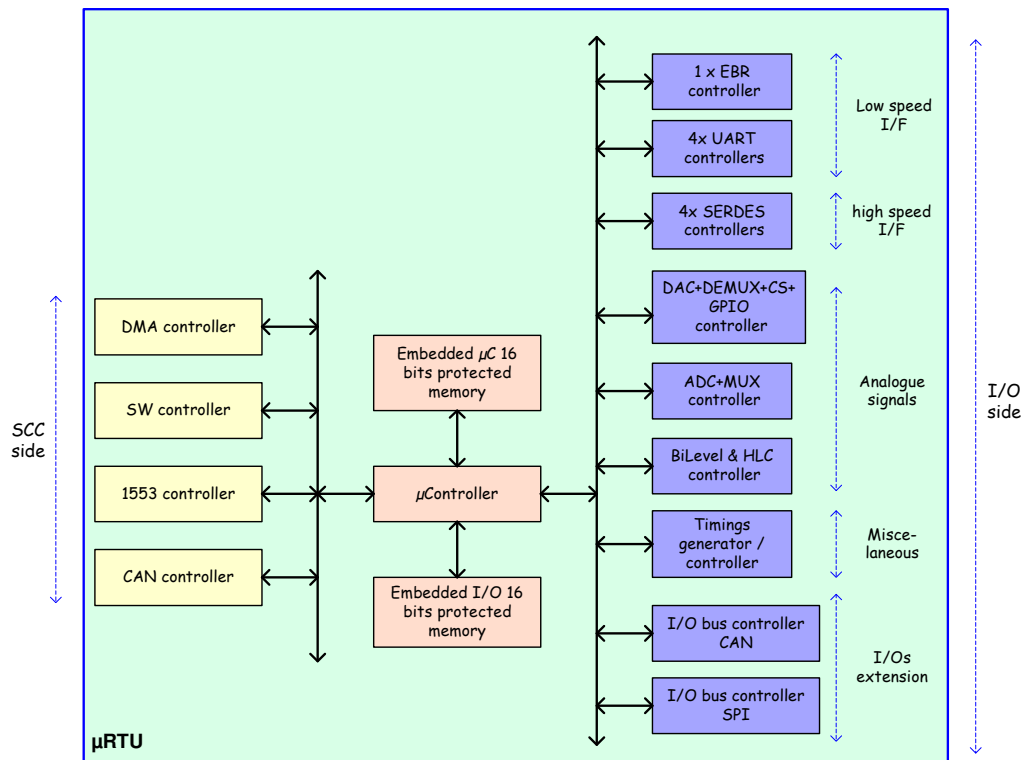
- HICDS should be modified to provide MIL1553 bus. It should also be of great interest to upgrade the HURICAN IP controller to include autonomous CAN management. Otherwise, upgrades shall be done externally with less efficiency.
- As for low-speed link, HICDS should also be modified to provide SpaceWire links.

3.3.2 RTU architecture

One RTU is composed of three basic modules that can be redounded or not:

- μ RTU
- Analogue and digital I/O modules
- Optionally a Power Converter depending if it is an embedded RTU in another unit

The RTU shall be highly flexible, very integrated and scalable to satisfy various applications simple or complex. Power supplies and analogue I/O of the RTU are summarised in their respective chapters. Based on trade-off, the μ RTU architecture part of the RTU is in accordance with the following block-diagram:



The ASIC budget to implement such a μ RTU is around 220000 gates and 220 functional pins fitting a 256 QFP package.

Power consumption is around 100 mW in stand-by mode and 1,2 W in active mode.

Total function with memories is estimated to 7000 mm².

3.3.3 SSR architecture

3.3.3.1 Memory parts types

The architecture and integration of a solid state recorder depend on memory parts. Main requirements of storage devices are:

- High integration density (in bits/cm², bits/g), resulting in lightweight memories with low Power consumption per access
- Fast access random to words/random to blocks.
- High data rate write/read.
- Low quiescent power consumption / No energy supply needed for data retention (~ non volatility).

Only a subset of memory technologies are relevant for the SSR namely:

- (1) SRAM, battery backed
- (2) DRAM, battery backed
- (3) FLASH EEPROM
- (4) FeRAM
- (5) MRAM

A brief overview of their main characteristics is given in following table. As already outlined in the introduction, battery backed SRAM/DRAM are suitable only for bridging of short power-off periods up to some days. This is not compliant with the envisaged data retention time of several years :

	Storage density	Random access time	Rate Retention time	Endurance	Radiation hardness
SRAM battery back-up	16 Mbit/cm ²	10 ns	Some days	∞	+/-
DRAM battery back-up	256 Mbit/cm ²	70 ns	Some days	∞	+/-
FLASH	1000 Mbit/cm ²	400 ms	10 years	Read = ∞ Erase < 10 ⁵	Storage: + Operating: +/-
Ferroelectric memory (FeRAM)	1 Mbit/cm ²	< 100 ns	30 years	Read/Write > 10 ¹⁰	Storage: + Operating: +/-
Magneto-resistive memory (MRAM)	32 Mbit/cm ²	< 100 ns	∞	∞	Storage: ++ Operating: +/-

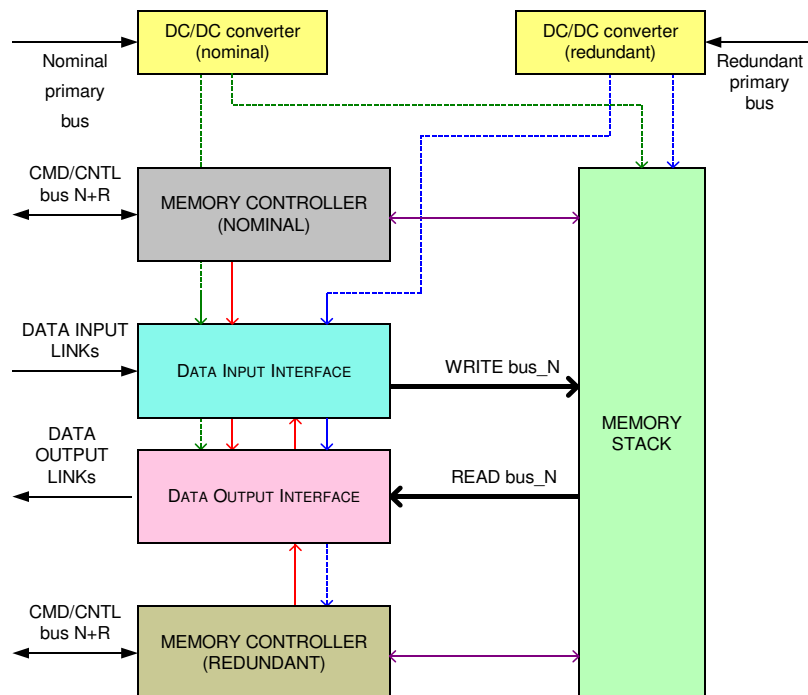
The emerging technologies FeRAM and MRAM are still not established, and it is still uncertain whether they will reach multi-source mass production status. FLASH is regarded to be the currently only technology which combines high storage density and non-volatility without the drawback of battery back-up. Both have bad integration factor to implement several hundredth of Gbits high storage density units

DRAM still remains the better solution to implement several hundred of Gbits. 512 Mbits is the current baseline while 1 Gbits will be in 1 year.

3.3.3.2 SSR architecture trade-off

The main architecture drivers of the SSR architecture (reference following block-diagram) are:

- Memory stack capacity
- Memory stacks modularity for redundancies and modularity/scalability.
- Input/Output data throughputs
- BER performance
- Budgets (mass, power, volume)



Two Memory controllers manage the memory stack from commands of the host computer.

One data input and one data output interfaces control the flux and integrity of data with the memory stack. Both interfaces can work simultaneously. Cumulated throughput can be up to several Gbits/s.

One memory stack can contain 256 Gbits or more depending on memory part size. The modularity can be 64 Gbits or less down to 8 Gbits. Data are organized in files with sectors. All sectors of the memory are available to the user. The management of files is under control of an integrated firmware located in the memory controllers.

Input/Output interfaces exchange data through 2 separate read/write buses.

One cold redundant power converter distributes the power to the SSR.

For AURORA, the implementation depends on the size of the board. With 6U boards, we 5 – 6 boards will be necessary :

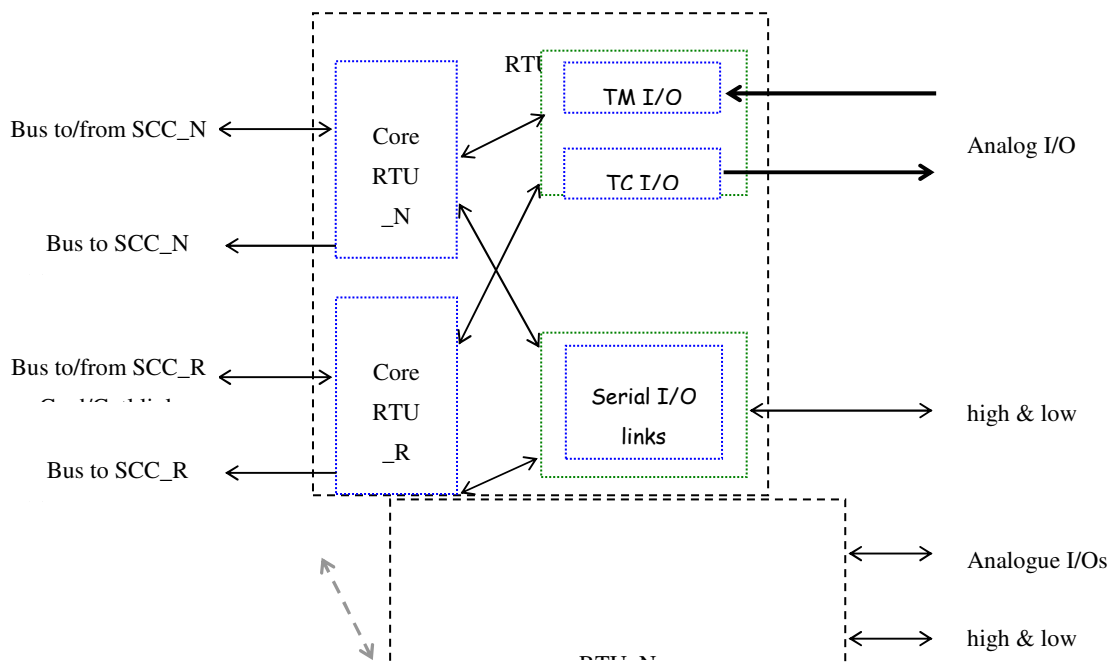
- One board containing the redundant processor function
- 3 boards containing 256 Gbits EOL (3 x 96 Gbits = 288 Gbits) more one additional board depending on reliability.
- One power converter board

3.3.4 PSU architecture

The implementation solution of the PSU depends on the P/Ls needs and I/O allocations which are unfortunately not available in URD.

The PSU architectures implementation leads to first solution with duplication of RTU module including I/O blocks and second solution with one redounded central core RTU and duplication of I/O blocks.

Both solutions can be implemented. The second solution is the current solution of most of platform systems. Nevertheless, thanks to a better integration of functions and to have a better modularity, the 1st solution is preferred for AURORA because the RTU can be either integrated in the PSU or in the P/L without modification of software and performances.



The PSU architecture includes redundant links between the SCCs and the core RTUs. The core RTU is redounded. One core RTU controls several I/O functions through simple sensor link like SPI, one-wire, I2C or other. I/Os are cross-strapped to the 2 core RTUs. Nominal and redundant power supplies are also cross-strapped on I/Os. The I/O functions are not redounded. I/O cross-strapping could be handled by different I/O number acquisition or command.

One RTU i module can be embedded in its P/L or in the SCC. The core RTU is based on FPGA or ASIC, while I/O are analogue parts based on discrete or analogue ASICs.

The size of the PSU is driven by the connectors. Assuming 4 connectors per 6U size board, one PSU handling 20 P/Ls can be implemented in 5 x 6U boards for RTU function more one DC/DC board resulting in 6 x 6U boards.

3.3.5 Analogue I/O definitions

AURORA I/O interfaces as describes in the URD are the following:

- Digital I/O high speed
- Digital I/O low speed
- 128 high-level commands
- 64 bilevel commands
- 64 heater commands
- 2 x 48 deployment commands
- 128 analogue signals acquisition (voltage)
- 2 x 64 + 64 thermistors acquisition
- 32 bilevel status acquisition

In addition, GNC/AOCS embeds the following equipments:

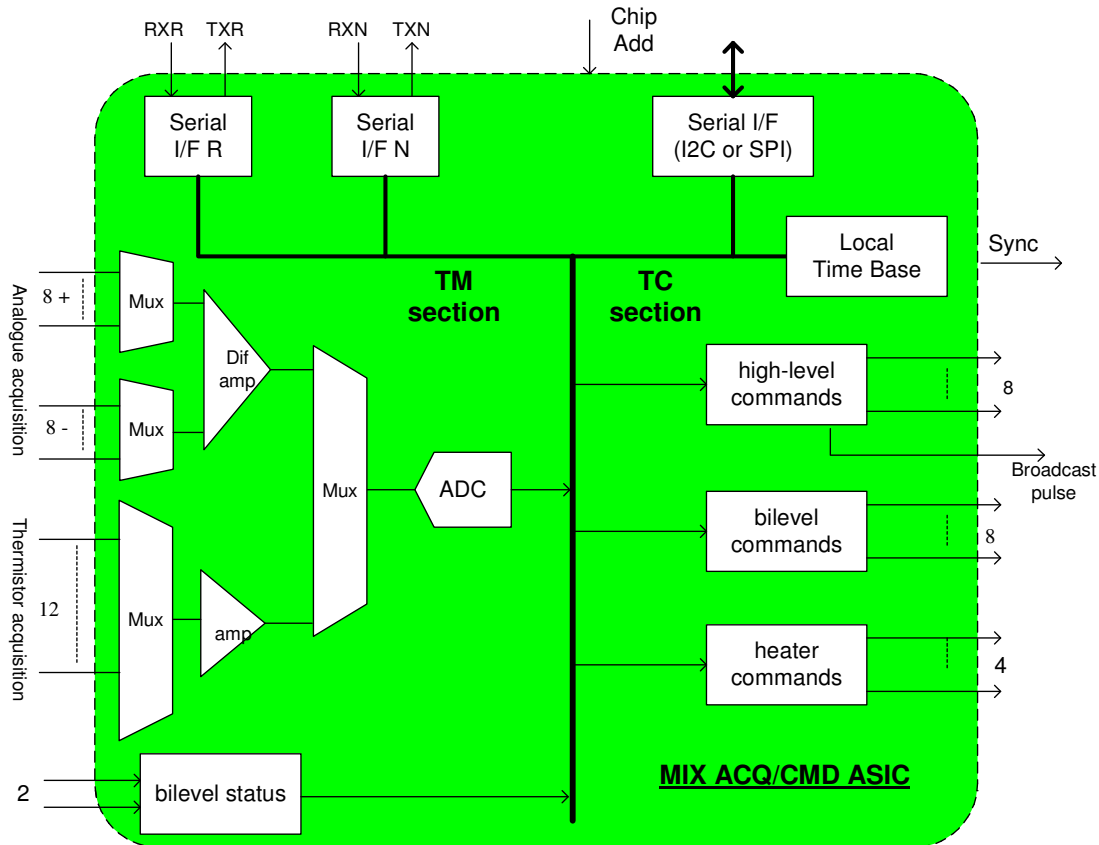
- Inertial Measurement Unit with gyro detection axes per channel, and 3 accelerometer detection axes per channel
- Redounded star tracker acquisition
- Accelerometer acquisition
- 4 x Sun sensors acquisition
- Reaction wheels control (x 4 orbiter) or (x 6 launchers)
- Solar Electrical Propulsion control (through central interface unit) (hypothesis : HLC type)
- Chemical propulsion system control, featuring between redounded to 24 self-redounded thrusters (hypothesis: HLC type)
- Chemical propulsion control (hypothesis : HLC type)
- Chemical propulsion gimbal mechanisms control (hypothesis : HLC type)

I/O Implementation is subjected to technology characteristics and availability but also to the development and recurrent costs. Some companies can be of interest:

For Mixed A/D ASIC design there are as a minimum Aurelia Microelectronics (Italy), Sidsa (Spain), STM (France with foundry in Italy), IMEC (Belgium), Dolphin (France), ATMEL (France), Raytheon (UK). Their libraries shall include op amplifiers, comparators, stable band gap voltage references, multiplexers, and voltage regulators as a minimum that must be hardened.

For MCM/Hybrid implementation, there are AME A/S (Norway), Astrium (France, Velizy), Lewicki (Germany), and 3D-Plus (France). MCM/hybrids are penalised by high development & recurrent Cost.

For AURORA, the best solution would be the implementation of standard I/Os within an ASIC. This one can contain the following functions to cover the overall need:



As conclusion, the I/O interfaces analysis for AURORA shows that the future activity shall be focused on the 3 following major points in order to miniaturize electronic.

- To develop a generic mixed analogue/digital ASIC or a generic analogue ASIC
- To select new more integrated commercial parts to be evaluated under space environment radiation
- To develop new analogue parts on rad-hard or rad-tolerant technologies as far as possible compatible to commercial parts (ADC, DAC equipped with serial bus (SPI, I2C, One-Wire), operational amplifiers, comparators, thermostat)
- To qualify passive part very low size packaging associated currently not existing for certain values (e.g. CMS capacitor CC0705 100nF instead of CC2210 or resistor RR0402 10k instead of RR0705) to have a better integration of analogue functions

3.3.6 Power supply solutions

Miscellaneous trade-off analysis lead to the following hypothesis concerning the voltages and power of the different power rails that shall deliver a power supply module:

Primary	20 to 35V
Secondary 1	5V
Secondary 2	3.3V
Secondary 3	2.5V
Secondary 4	1.8V

The secondary output power estimated is as follows:

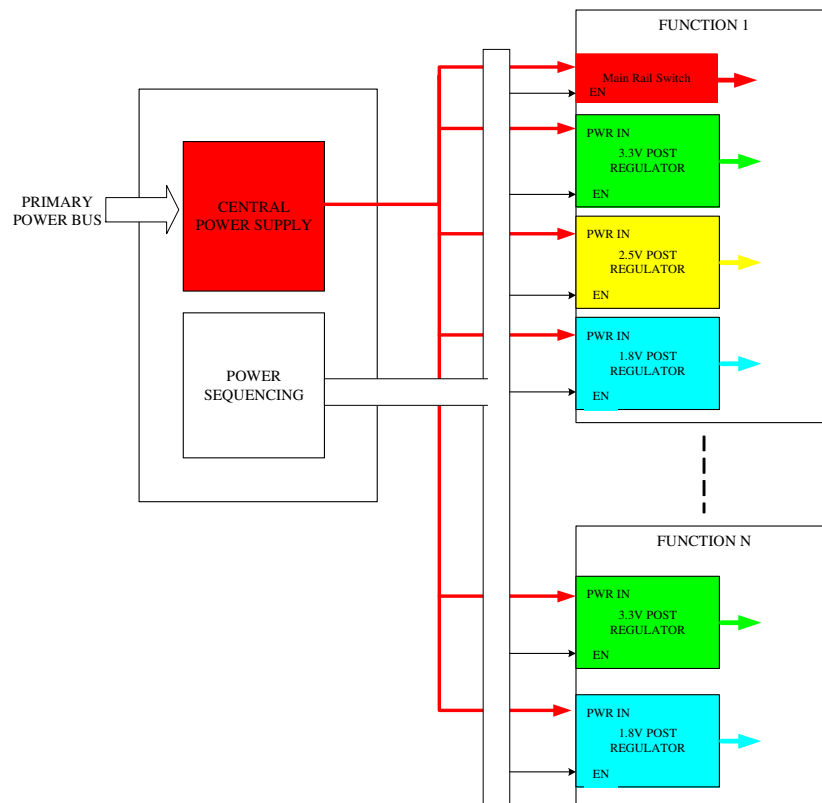
Located in the main unit:	15W Max
Located in other units	4W Max

The average power consumption shall not exceed 20W for the most demanding application.

Some key points shall be considered for the architecture :

- The accuracy of the secondary rail shall be better than 5%, including load transients. This requirement corresponds to an accuracy of 90 mV on a 1.8 V rail.
- The architecture shall optimize the efficiency for a maximum 20W primary power dissipation of a unit.
- The architecture shall be flexible to accept a wide range of loads and also optimize part count.
- The different secondary rails shall meet sequencing constraints during start-up and shutdown in order to prevent logic parts stress.
- Power supply shall offer the possibility to disconnect a failed function from the power bus.

Following architecture can thus be envisaged:



The central power supply purpose is to:

- Convert the primary unregulated power bus is a fully regulated secondary rail available for all avionic functions
- Provide an interface with the primary power bus compatible with the EMC requirements including primary to secondary insulation.
- Provide the required protections required to prevent failure propagation to the power bus and to the down stream functions. (UVD/OVD/ SSPC)

The secondary voltage shall be selected in accordance with the following criteria:

- The power distribution of this rail to the different functions shall not affect the accuracy performance (5%) (i.e. maximum voltage)
- This secondary rail shall be as far as possible usable as is by the different function
- It shall not be too high in order keep post regulation efficiency acceptable.

As a conclusion, the architecture proposed is based on a main converter that provides single regulated secondary rail which is distributed to all unit sub-functions. The maximum power consumption on this rail is supposed to be lower than 15W.

Each sub-function embeds one or several post-regulators providing low voltage rails.

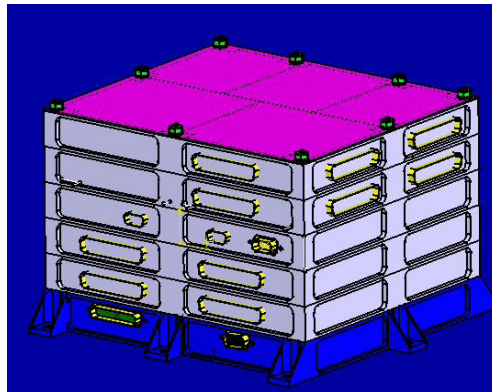
Studies shall be done to design these post regulators and the main converter that can be partly based on commercial parts or on specific designs to be implemented on mixed analogue ASIC.

3.3.7 Packaging solutions

AURORA On electronic units shall be based on a modular concept packaging because of the various numbers of applications. The modular packaging solutions are driven by mass, adaptability to different missions, I/O connections number, testability and cost.

The module that constitutes the unit, shall comply with an integrated electronic whose maximum area is about 15000 mm². With connectors and power supplies, it is about 30000 mm². A 3U format solution can be selected and preferred. The 6U format also seems a good solution but less efficient to implement in small spacecraft. Nevertheless, these two formats should be considered to permit versatility in packaging for the 3 kinds of applications (Orbiter, Lander, Rover).

The mechanical box standard is an assembly of modules stacked or piled together by means of tie rods. The internal interconnection is done through a back plane, which can be an external interconnection to ease the thermal dissipation. The figure below provides an overview of the mechanical concept. A full study shall be made to design a qualifiable model.



For important thermal dissipation in small volume, thermal exchange systems as heat pipe or fluid loop shall be implemented. Current designs are not compatible of AURORA specifications and some efforts of miniaturization of the fluid loop shall be done.

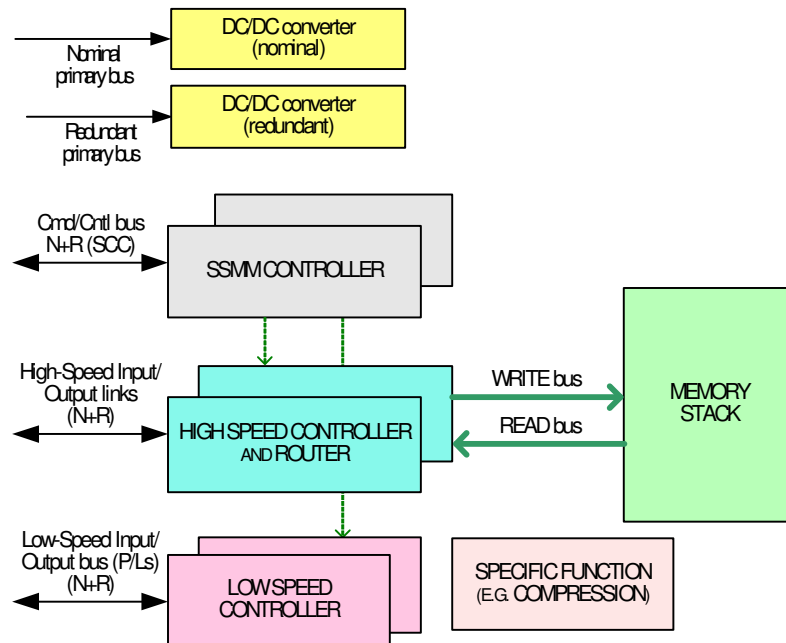
As a conclusion, the packaging studies shall be focused on following major points:

- The interconnection with the:
 - Development of high density interface connectors with a reduced size,
 - Development of miniaturized surface mounted connectors,
- The component technology miniaturization with:
 - The qualification of high density package like BGA, CSP and associated high density PCB,
 - The development and the qualification of system in a package,
- The thermal design with the development of miniaturized heat fluid loop.
- The mechanical design for the modular approach:
 - Development of a method and a tool to analyse the equipment behaviour;
 - Development and qualification of a technology to harden the component against this kind of load.

3.4 Unit design specifications

3.4.1 SSR specification

SSMM functional block-diagram is the following:



Main functions of the SSMM are:

- data packets storage from SCC, PSU and P/L through high and low speed links
- retrieval to SCC and TM through high speed links
- ciphering function
- configurability through a low speed bus
- SSMM architecture implementation can also accept additional specific functionalities like a compression, packetisation, de-packetisation functions which will be connected to the routing function. This specific function shall be embedded in a reprogrammable function tightly coupled to the SSMM controller.

SSMM implements:

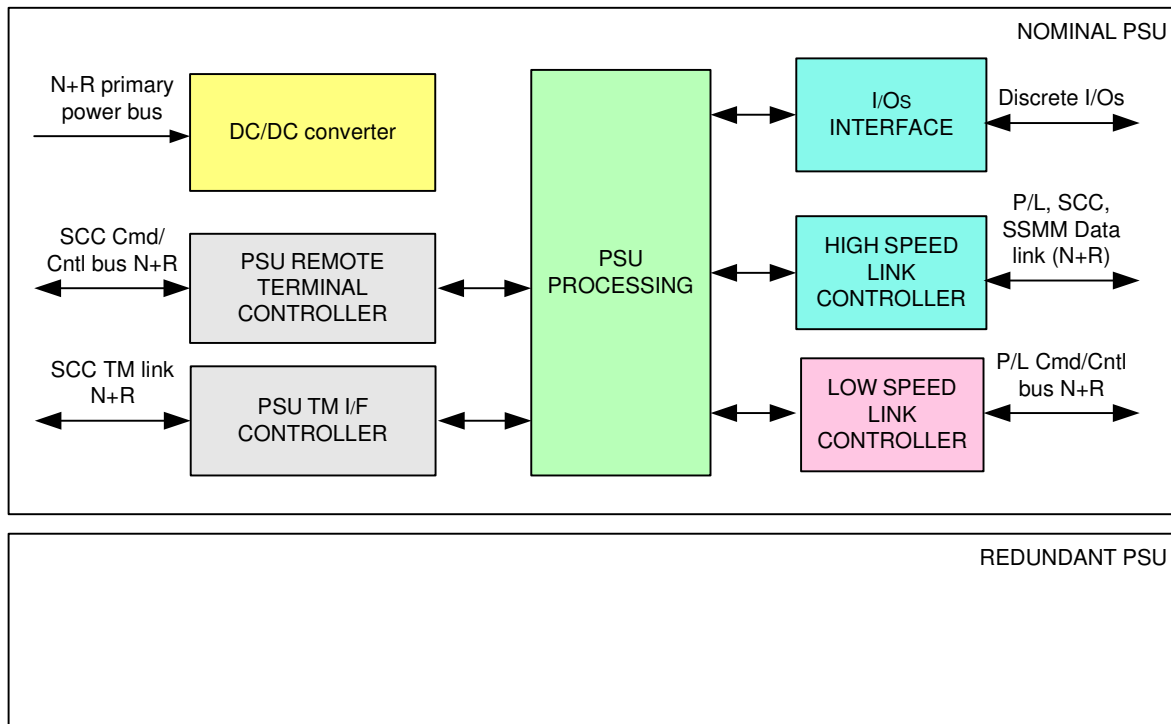
- a DC/DC power supply
- an high-speed link controller router
- a low-speed link controller
- an SSMM controller
- a modular memory stack whose minimum size is 64 Gbits with a 64 Gbits modularity. No maximum is given
- optionally specific functions like ciphering, image compression,

SSMM main requirements:

- Interfaces:
 - SSMM shall provide/receive data from 8 x nominal/redundant high speed SpW links
 - SSMM shall accept command/control from the nominal/redundant low speed MIL STD 1553 bus
 - SSMM shall be connected to the nominal/redundant AURORA primary power buses
- Memory:
 - SSMM shall offer memory stack (one physical module) configuration for up to 8 users with a sector granularity (smallest quantum to read or write – size 2, 4 or 8 Mbytes)
 - SSMM shall manage files with a file identifier
 - SSMM shall be able to simultaneously record and read files over the 8 channels
 - SSMM shall automatically scrub and correct data words of the memory stack to fulfil the BER over short-term and long-term (mission lifetime) duration
 - SSMM shall implement an auto-test function
 - SSMM shall provide a minimum memory stack slice of 64 Gbits BOL
 - SSMM shall provide a memory unit modularity of 16 Gbits
- Performances:
 - BER of the memory stack shall be lower than 2×10^{-10}
 - SSMM shall fulfil all its performances over 15 years in orbit (all powered modes)
 - SSMM power consumption shall be lower than :
 - 10 W in retention mode
 - 25 W in read/write modes
 - SSMM mass shall be less than 4 kg

3.4.2 PSU specification

PSU functional block-diagram is the following:



PSU supports up to 20 P/Ls (4 high-speed P/Ls and 16 low-speed P/Ls)

Functional interfaces of the PSU can be summarised as follows:

- One low-speed cmd/cntl communications link with SCC at a maximum data rate of 1 Mbit/s
- One high-speed data communications link via a router with SCC or SSMM and 4 x P/Ls at a maximum data rate of 100 Mbit/s (5 x 20 Mbit/s)
- One low-speed cmd/cntl communications link with P/Ls at a maximum data rate of 1/2/4 Mbit/s
- Discrete analogue I/O signals with all P/Ls

PSU main requirements:

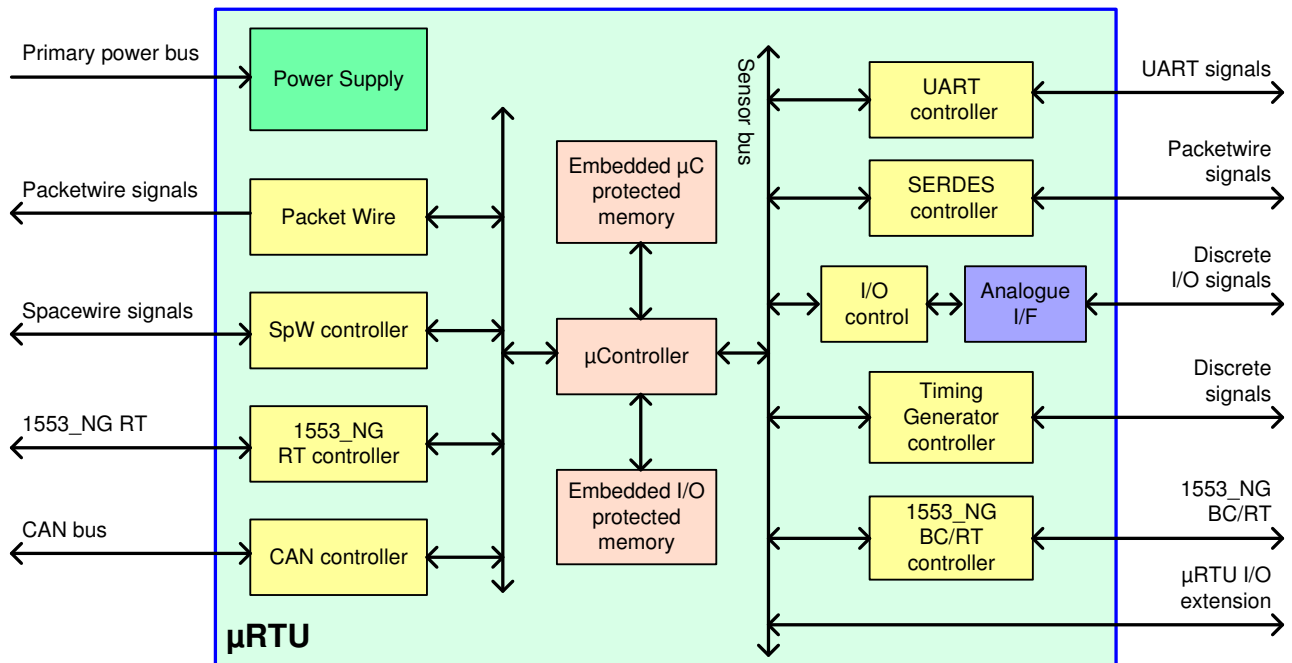
- Interfaces:
 - PSU shall provide one nominal/redundant SpW high-speed link allowing to exchange data with the SCC, the SSMM and 4 x P/Ls through a router located outside the PSU
 - PSU shall accept command/control from the nominal/redundant low speed MIL STD 1553 bus
 - PSU shall command and control P/Ls through a nominal/redundant low-speed 1553_NG bus
 - PSU shall interface with following TM/TC nominal/redundant basic analogue signals for one P/L/
 - 1 Temperature acquisition
 - 2 Analogue acquisitions

- 2 Bi-level Status acquisitions
 - 1 Relay status acquisition
 - 1 Standard Discrete Input
 - 1 Standard Discrete Output
 - PSU shall be connected to the nominal/redundant AURORA primary power buses
- Functionalities:
 - PSU shall embed a SPARC processing function
 - PSU software shall work on a programmable RTC clock
 - PSU shall control up to 32 users even though it is tailored for 20 P/Ls
 - PSU shall implement an auto-test function including analogue I/O tests
- Performances:
 - PSU shall fulfil all its performances over 15 years in orbit (all powered modes)
 - PSU power consumption shall be lower than :
 - 2 W in stand-by mode
 - 10 W in active mode
 - PSU mass shall be less than 3 kg

3.4.3 μ RTU specification

RTU is based on several μ RTU assembled in the same unit.

μ RTU interfaces up to 4 peripherals. Functional block-diagram and interfaces of the μ RTU can be summarised as follows:



It is possible to implement several μ RTU through the μ RTU extension bus.

μ RTU shall have the following main functionalities:

- on controller side (SCC or another one):
 - a nominal/redundant 1553_NG RT interface
 - a nominal/redundant CAN interface
 - a nominal/redundant SpW interface
 - a PacketWire interface to the TM function of the SCC
- A μ controller with its program memory and I/O data memory
- A μ RTU shall address up to 4 peripherals and provide the following services for one peripheral:
 - 1 x UART interface
 - 1 x Packet Wire interface
 - 1 x set of discrete I/O interfaces:
 - high-level commands
 - bi-level commands
 - bi-level status
 - differential analogue voltage, current and temperature acquisition

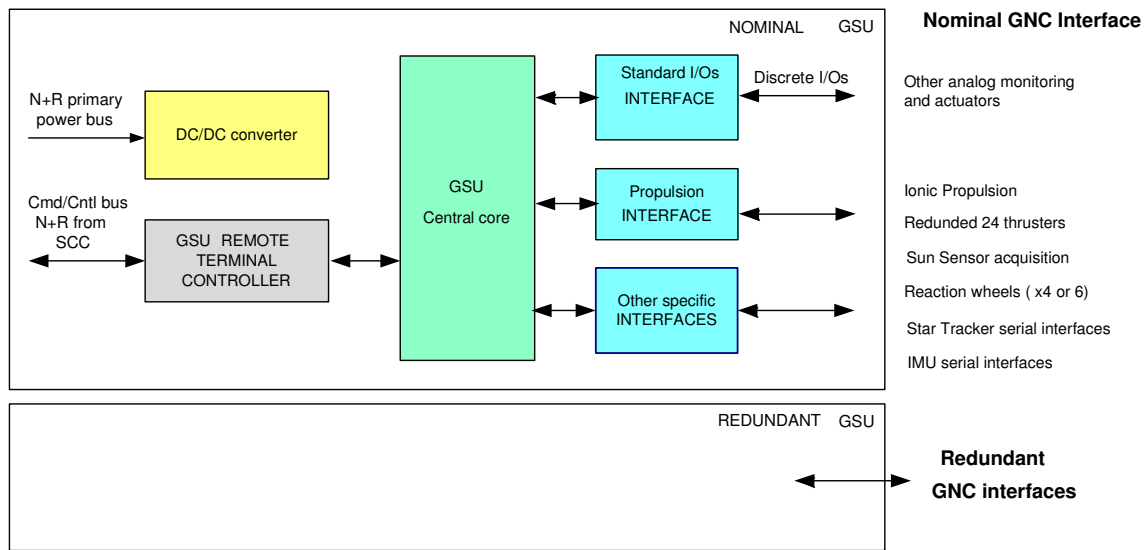
- 1 x timing manager
- 1 x nominal/redundant 1553_NG BC/RT interface
- An Internal Sensor Bus interface allowing to extend I/Os
- An optional DC/DC converter for a stand-alone use

μRTU main requirements:

- Interfaces:
 - μRTU shall implement a nominal/redundant 1553_NG RT bus interface to SCC
 - μRTU shall implement a nominal/redundant CAN bus interface
 - μRTU shall implement 3 x SpW bus interfaces
 - μRTU shall be connected to the nominal/redundant AURORA primary power buses
 - μRTU shall interface with following nominal/redundant basic analogue signals for one peripheral
 - 4 x analogues inputs (including temperature acquisition)
 - 2 x bi-level status
 - 2 x bi-level commands
 - 2 x high level commands
- Functionalities:
 - μRTU shall embed a SPARC processing function
 - μRTU software shall work on a programmable RTC clock. Daily drift shall be better than ± 10 ppm over 1 day for the min-max operational temperature range including a $\pm 10^{\circ}\text{C}$ temperature variation
 - μRTU shall implement an auto-test function including analogue I/O tests
- Performances:
 - μRTU shall fulfil all its performances over 15 years in orbit (all powered modes)
 - μRTU power consumption shall be lower than :
 - 0,1 W in stand-by mode
 - TBD W in active mode
 - μRTU mass shall be less than 150 g

3.4.4 GSU specification

GSU functional block-diagram is the following:



GSU main requirements:

- Interfaces:
 - GSU shall provide/receive at least the following standard acquisition interfaces:
 - Remote Terminal interface on 1553_NG Cmd/Ctrl system bus
 - 20 Temperature acquisitions (TH) dedicated to GNC/AOCS thermal control, TBC
 - 20 Temperature acquisitions (TH) dedicated to GNC/AOCS internal temperature (housekeeping), TBC
 - 32 GNC/AOCS Analogue acquisitions (N+R) (ANA) TBC
 - 20 GNC/AOCS Bi-level Status (N+R) (BLS) TBC
 - 20 GNC/AOCS Relay status (N+R) (RS) TBC
 - 20 GNC/AOCS Standard Discrete Input (N+R) (SDI) TBC
 - GSU shall provide at least the following standard command interfaces:
 - 20 High Power Relay Commands (N+R) (HPRC), TBC
 - 20 standard Discrete Output (N+R) (SDO), TBC
 - GSU shall provide at least the following miscellaneous interfaces:
 - The GSU shall provide Chemical Propulsion interface
 - GSU shall provide Low level drivers command for Ionic Propulsion

- GSU shall provide at least 4 Coarse Sun Sensor (CSS) interface
- GSU shall provide at least 1 Star Tracker (SST) interface
- GSU shall provide an IMU interface
- GSU shall provide at least 4 Reaction Wheel (RW) interfaces for orbiter and 6 Reaction Wheel (RW) interfaces for launcher

- GSU shall accept TM/TC commands from either a nominal or redundant 1553_NG bus PSU shall be connected to the nominal/redundant AURORA primary power buses
- GSU shall be powered from either a nominal or redundant primary power bus

- Performances:
 - PSU shall fulfil all its performances over 15 years in orbit (all powered modes)
 - PSU power consumption shall be lower than :
 - 1 W in stand-by mode
 - 5 W in active mode
 - PSU mass shall be less than 4 kg

3.5 Basic SW and Services

3.5.1 SW user requirements

3.5.1.1 Software systems functions

Throughout the study, the SW definition has been derived from the Aurora avionics functional specifications written in phase 1 as well as from the experience of similar science missions such as Rosetta/Mars Express/Venus Express.

The main functions of the avionics system are under the control of the software applications of a central computer (the central on-board software), in particular:

- DMS (Data Management System : TM/TC management, System INIT , SAFE mode, System Reconfiguration...),
- AOCMS (Attitude and Orbit Control and Monitoring System),
- Power,
- Payload management,
- Platform Management,
- Thermal control,
- FDIR (Failure Detection Isolation and Recovery)

3.5.1.2 Generic overall architecture

In the current systems, there are few commonalities between the central software and the other pieces of software disseminated in the other units. This implies that :

- the high level software applications must have the detailed knowledge of the way the data bus(es) is/are operated,
- the architecture of applications software strongly derives from the I/O management architecture.

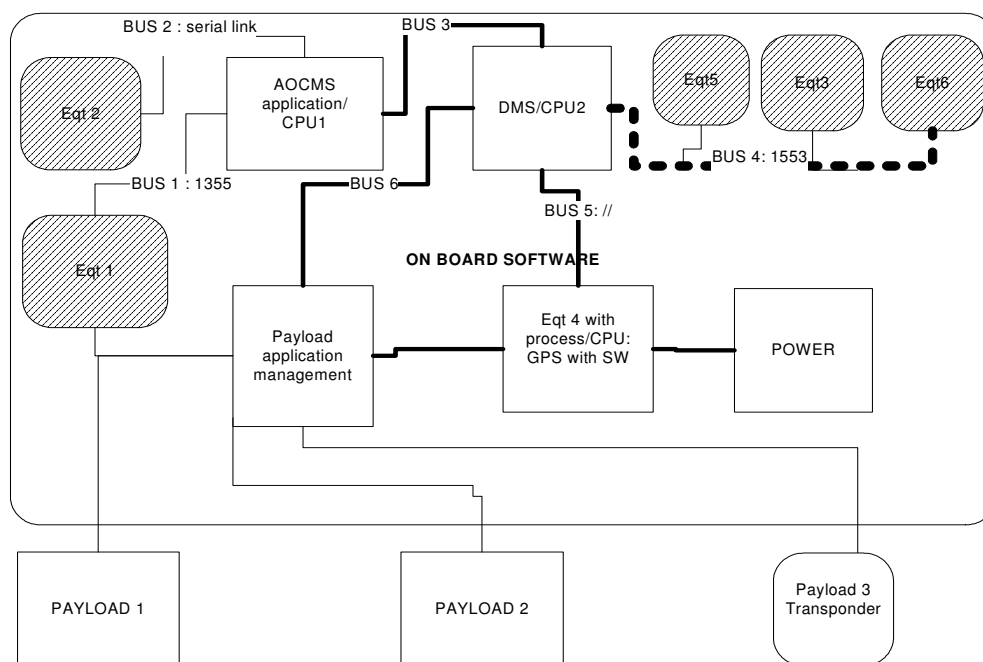
This makes difficult to reuse software from one mission to another (and even worse from one class of vehicle to another) because most of the code and even its overall architecture are very specific.

In future systems, the modularity and the level of standardization of the software required in centralized architectures need to be improved. Moreover, the complexity and the level of autonomy of the planetary exploration missions are continuously increasing. Even taking into account the progress of the flight computer technology, the processing power available in a single computer may no longer allow keeping a fully centralized architecture. Therefore, the future of on-board systems will be probably based on more complex architectures, including distribution schemes:

- Software applications distributed on multiple computing nodes (processors, sensors, actuators, payloads, equipments), across different buses and networks,
- Complex functions requiring the cooperation of several computing nodes,
- Management of the redundancy of the processors and of the other units, in order to ensure fail operational behaviour of the overall software during the most critical phases
- communications with both “dumb” equipment (no software inside) and “intelligent” equipment (more or less complex software inside).

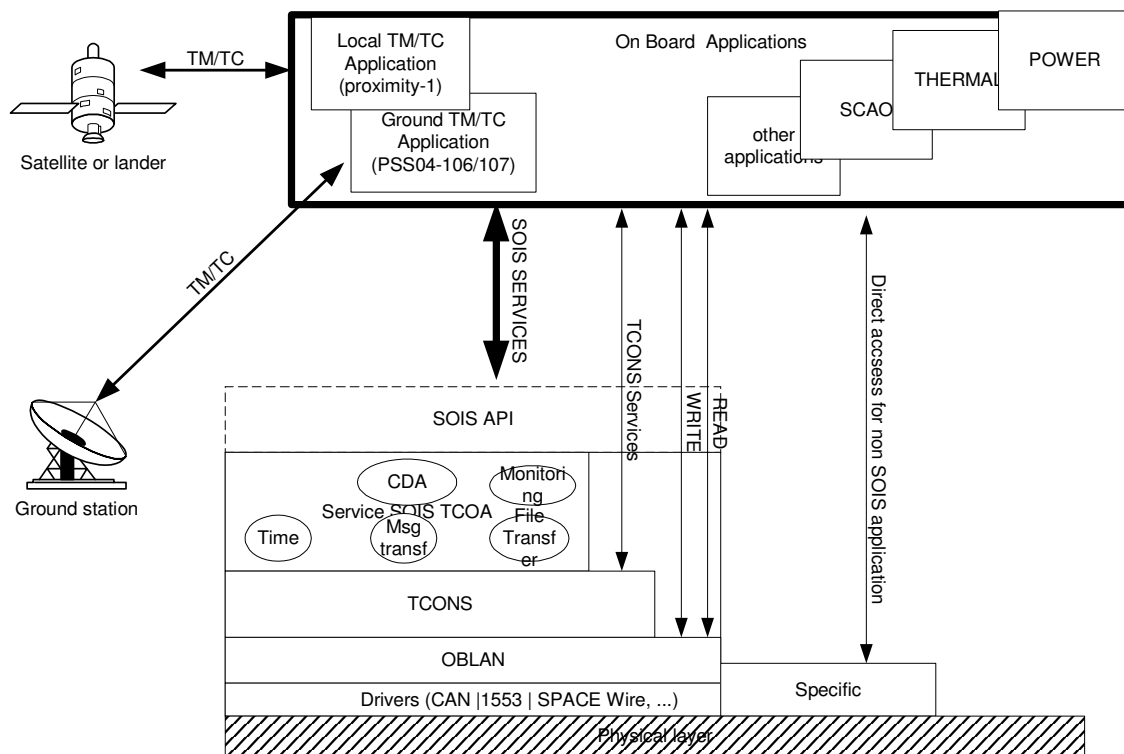
Ideally, all the application software in the system should use standard services to communicate with both the dumb equipments and other applications running in intelligent units whatever their function is. Moreover, the way this communication is managed by the applications should be independent from the nature of the physical links and the overall topology. For example, it should be possible for an application software to communicate in the same way with a sensor connected directly to the computer in which it is running and with another similar sensor that is accessible only via one or more intermediate nodes.

An example of a distributed architecture is presented in the figure hereafter. The on-board application software is made of several processes distributed on different nodes. The allocation on the processes on the nodes is done on a functional basis (the nodes remains rather “specialized”). The nodes are connected each others through one or several buses or point to point links.



3.5.1.3 External and On-board communications

The CCSDS inter-agencies organisation provides a set of communications standards that allow for inter-operability of space systems. The applications in charge of the management of the external communication have to comply with the CCSDS standards. The TM/TC applications (local and/or ground communication) receive TC from the ground and/or from local satellite; and send TM to the ground and to a local satellite. Accordingly, the communication management applications translate an external communication protocol ground/On-board protocol (PUS) into an on board/on Board (SOIS) protocol. They may interface with the SOIS stack at different levels. The figure below summarizes the interactions between the applications and the standard services. The other applications (AOCMS, Thermal, Power ...) use the TCOA services API for all the commands and data exchanges, the lower layers if required (especially when specific hard real time constraints cannot be met using the standard stack).



Derived from the software user requirements [SW-URD], one of the most important implementation constraint for the Basic SW is to provide the application with standard services through an Application Programming Interface (API) that ensures the compatibility with the future CCSDS SOIS standards (Spacecraft Onboard Interfaces and Services). This will hide the SW lower layers and hardware detailed implementation which is necessary to allow the underlying technology upgradeability to face obsolescence problems with minimized impacts on the system applications as well as to provide the possibility to increase performance and functions through new technology.

SOIS define services based on standard communication protocols between several spacecraft elements at hardware and software level. It uses the network OSI terminology model to define the SOIS layers:

- The data bus (or network) physical implementation (OSI physical layer, level 1),
- The Data link layer implementation (OSI link layer, level 2)
- Protocol implementation in network layer and transport layer (OSI Network layer level 3 and OSI transport layer level 4)
- SOIS services in application layers (OSI Application layer, level 7)

The Basic software shall be considered as a structured library of modules providing services to higher level application software. Most services are derived from the SOIS standards, but not all.

3.5.2 Basic SW Preliminary Design

The basic software is part of the Aurora toolbox and defined as being the generic set of lower level software that should be used across various vehicles involved in the Aurora mission.

The Basic SW design aspect have been studied during phase 2, deriving SW User requirements [SW-URD] into preliminary design specifications [DS-BSSS] that takes place within the avionics toolbox. This document contains the Design Specification for Basic Software and Standard Services of the Aurora Avionics Architecture System. A Unified Modelling Language (UML) tool has been used to define the Basic SW Services in support to this design specification.

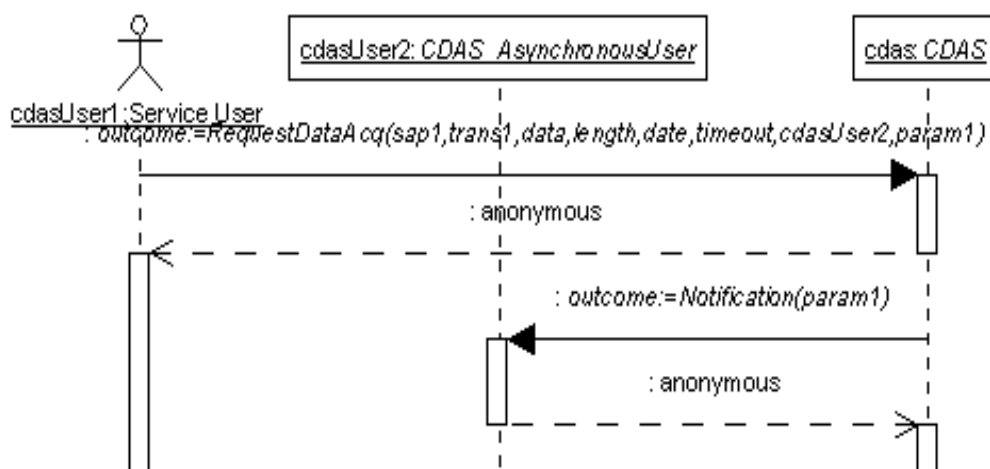
A description of the UML model for the three services of the Basic Software and Standard Services has been provided during this activity:

- Command and Data Acquisition Service (CDAS)
- Message Transfer Service (MTS)
- Time Distribution Service (TDS)

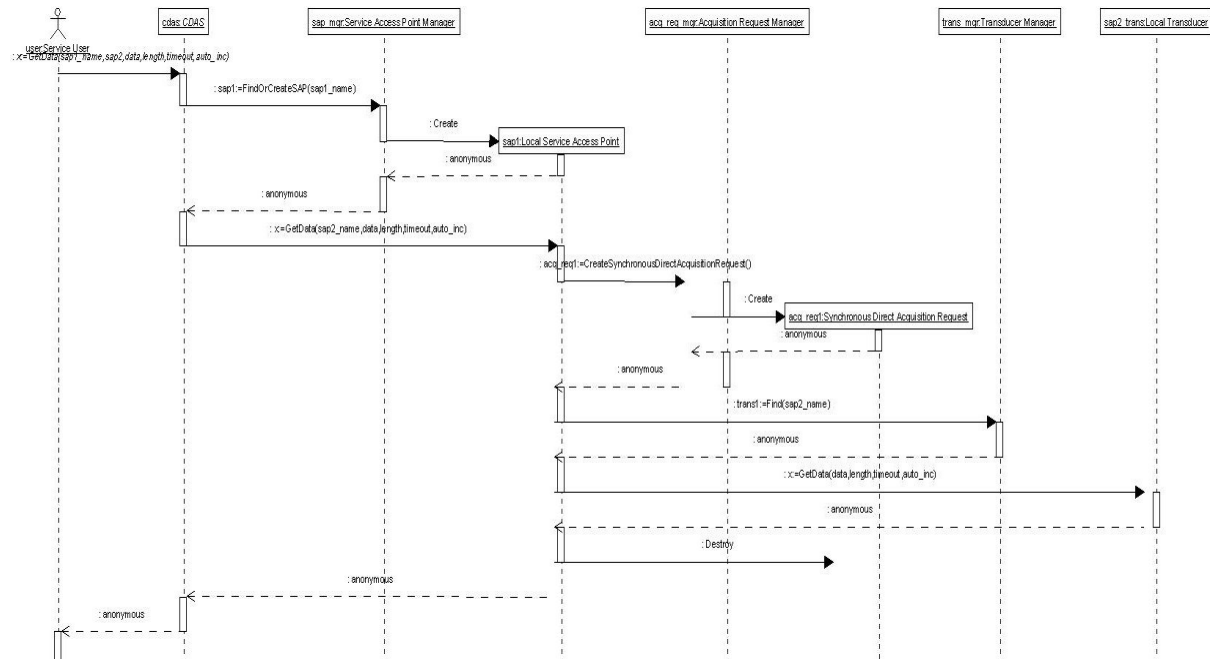
The [DS-BSSS] document is split into a description of general Use Cases scenarios and Packages. Within each package, Sequence Diagrams describe how each Use Case is implemented and the Class References describe the classes that implement the Package.

As an illustration of such sequence diagram, the figure bellow provides the use case diagram for the service “Asynchronous Direct Data Acquisition” (CDAS). In this use case, the Service User, cdasUser1, invokes CDAS to asynchronous directly acquire data from a sensor, trans1. Control is returned immediately. When the data has been acquired, notification is send to the specified Service User, cdasUser2.

All the considered use case for Basic SW Services are discussed in detail in the [DS-BSSS] document.



The Scenarios are further detailed through sequence diagram. For instance, we have extracted in this report the capture of the scenario of synchronous direct acquisition of data from a sensor directly attached to the processor with the corresponding explanations.



1. user invokes the GetData method on the CDAS interface. The FindOrCreateSAP method of the singleton Service Access Point Manager object, sap_mgr, is invoked to find the Service Access Point instance for user. One is not found and so, because the SAP address of user1 is local, a Local Service Access Point object (sap1) is created and its GetData method invoked.
2. sap1 invokes the CreateSynchronousDirectAcquisition method of the the singleton Acquisition Request Manager object, acq_req_mgr, to create a Synchronous Direct Acquisition Request object acq_req1.
3. sap1 invokes the Find method on the singleton Transducer Manager with an argument of the SAP address of the sensor 2. This finds the existing Local Transducer object (sap2_trans2) because the SAP address of sap2 matches and a reference to this is returned to sap1.
4. sap1 invokes the GetData method on sap2_trans. This performs the sensor-specific data acquisition and returns the data to sap1.
5. sap1 destroys the Synchronous Direct Acquisition Request object and returns the data to user.

3.6 Technology road-maps

3.6.1 Overview

In order to comply with AURORA mission planning, at least four generations of avionics shall be considered:

➤ **2007 and 2009 missions**

The Aurora avionics core is based on existing avionics building blocks not fully compatible with the toolbox defined in the present study. Nevertheless, some Aurora building blocks like the new generation TM/TC ASIC developed in the framework of the HICDS study can be used to improve existing onboard computer products based on the ERC32SC microprocessor. In addition, the functions that must be developed for these missions shall use as far as possible the on-board interface standards selected in the Aurora toolbox.

➤ **2011 and 2014 missions**

The Aurora avionics is based on the new spacecraft controller core and peripheral modules, with mission and/or vehicle specific peripheral cores interfacing the existing hardware reused from Mars Express that cannot be replaced. (for example the inertial measurement unit that is not compatible with the standardized Aurora onboard communication standards). The avionics architecture remains centralized.

➤ **2018 missions**

Improvement of the integration of the functions (spacecraft controller core and peripheral interface cores) by developing more integrated SOC implementing the generic building blocks and by developing sensors and actuators directly compatible with the selected onboard communication standards (diminution of the number of mission specific peripheral modules).

➤ **Subsequent missions**

Modification of the data handling architecture to take benefit from the feasibility of a spacecraft avionics on a board, integration of highly miniaturized optical and inertial sensors at board level, use of transparent application distribution technologies with a very high level of fault tolerance.

3.6.2 Incremental Development approach

The proposed approach consists in an incremental development compatible with later availability of the user requirements:

- In a first step, only the very low level hardware design blocks are implemented (a design block is either a VHDL IP, either a basic design electrical schema). The basic software specific to each block is also developed (it is considered as a part of the function implemented by the block).
- In parallel, a development and test environment is defined to automate as far as possible the assembly of these blocks, and the validation of the larger building blocks obtained in that way. This environment supports platform based hardware-software co-design techniques allowing building quickly a virtual prototype of any system obtained by assembling these blocks. Such a virtual prototype can be used to characterize the performance of the systems (functional performance, mass/PCB surface, power consumption). It can be used also to support the early validation of the software applications developed for the system.
- A typical configuration of the avionics core is instantiated as a modular demonstration platform. The objective is to validate not only the basic blocks, but also especially the semi-automated assembly process and the virtual prototyping tool (by comparing its behaviour to the demonstrator).
- The interface of the toolbox development environment with the final step of the manufacturing process (mainly ASIC and PCB manufacturing) are also checked. Some complex hardware building blocks like the LEON2 processor that are not impacted by possible evolution of the user requirements can be even pre-developed as “hard IP”
- When there is enough confidence in the stability of the user requirements, the higher level building blocks like the complete spacecraft controller core are then designed by freezing a selected combination of the low level design blocks. This configuration is functionally validated with the corresponding basic software on the demonstrator, before the manufacturing of the ASIC and/or printed circuit boards.
 - The high level building blocks (the spacecraft controller core and the peripheral cores) are then qualified as independent products, and proposed as COTS equipments by their manufacturers.
 - The high level building blocks are now available in the building block library, but the low level design blocs remain also available to develop mission specific functions.

3.6.3 Road-Maps

As explained in the previous paragraph, the AURORA program will require the progressive development of several hardware, software building blocks, tools and technologies. The Road-maps provided below shows on a timescale the foreseen development of the required technology in the mid-term future.

3.6.3.1 AVIONICS SYSTEM ARCHITECTURE

Activities	2006	2007	2008	2009	2010	2011	Comments
PROTOCOLS SPECIFICATIONS							This covers the specification of protocols covered by the various working groups : "on-board bus & LAN", "time critical on-board applications & network services", "plug and play applications", "spacecraft transducer systems"
CO-DESIGN METHODOLOGY							formal & executable partitioning, hardware/software partitioning - library management, proof-based design validation, hardware - software automatic generation

3.6.3.2 ELECTRONIC TECHNOLOGY ROAD-MAP

Activities	2006	2007	2008	2009	2010	2011	Comments
ASIC 90 & 130 nm							- high speed digital ASIC - analogue ASIC
FPGA							- Large FPGA - FPGA for reconfigurability
DSP							- Next DSP hi-rel generation or Rad tolerant DSP core based on several DSP
MEMORIES (SSRAM, FLASH, FeRAM, MRAM, ...)							- Technology upgrade with DDRAM, MRAM, ...
LINKS (new 1553, PCI express, Gigalink, One Wire)							- New buses for unit internal links and between units for sensor link command/control link and data link
MCM reconfigurable							- In favour of standard product reconfigurable by user at ground or in flight. Based on a CPU core plus a reconfigurable part
PARTS PACKAGING REPORT							CGA, BGA, CSP high density packages for next applications

3.6.3.3 HARDWARE BUILDING BLOCKS ROAD-MAP

Activities	2006	2007	2008	2009	2010	2011	Comments
SPACEWIRE	■						- remote access IP - delocated router IP
μRTU (ASIC, core module)	■						
ANALOGUE ASIC	■						- cmd/monitoring ASIC - thermostat ASIC
Misc. MODULES	■						- memory stack - guidance I/O modules
Power MODULES	■						- central PSU - post-regulator - main DC/DC
MECHANICAL PACKAGING	■						- elementary module - unit (MSTH)

3.6.3.4 SOFTWARE ROAD-MAP

Activities	2006	2007	2008	2009	2010	2011	Comments
Industrialisation of Open Source COTS Software	■						
Development of Basic Building Blocks Library	■						
RTOS and Programming Languages	■						
Development Process	■						
Software Architecture Evolution		■					

3.7 Synthesis and recommendations

The ambitious Aurora program will experience a uniquely long duration time frame in the history of space exploration. This calls for an innovative approach in the analysis of the drivers that will be dimensioning factors for its technical feasibility over the full timescale of the Aurora Missions. Indeed, a classical approach for definition of the avionics system performed using the reference of a single mission with empirical re-use of avionics element to next mission for different spacecrafts and system functions would lead to a variety of potentially non-homogenous designs and technology development at a probable high cost.

This assumption is therefore that the key enabling factor will not be mainly development of products, increasing performance and added new technology but also the capability to define and upgrade an open modular architecture with a standardised set of building blocks implementing data management and communication services. Functional modules designed within this frame will ensure avionics upgradability with no or low impacts to the global system concept. New functions will be integrated into the existing system at the rhythm necessary to cope with the new missions objectives.

Modular Architecture and building blocks

Starting from the experience gained through missions such as ROSETTA, Mars express and Venus Express and taking into account the pre-development activities of the Highly Integrated Core Data System (HICDS) performed on the Bepi-Colombo reference mission, the A3SysDef study has confirmed the high interest of this concept. As a practical output, an open architectural structure has been provided along with the preliminary design specifications for functional building blocks that are deemed necessary to perform the first Aurora missions (ExoMars and Mars Sample Return).

Data processing technology

First iteration on the implementation study as been taking a technology reference background using the most advanced electronics and standardisation works developed for being used within space avionics systems. This concerns for instance the electronic components technology (e.g. Leon processor, System of chips, latest ASIC and FPGA technology), the on-board communication data links and standards (SpaceWire, Can, 1553, Sensor bus, CCSDS/SOIS) and software developments (Rtems operating system, Data Management Service library).

Improvement of the development techniques

The study has also made clear that the efficiency of such approach will be improved thanks to an adequate usage of associated recent methodologies and tools for HW/SW systems such as UML, Co-Engineering, Co-Design and Co-Simulation which become essential to the definition, development and validation of complex and integrated data systems. As such, these engineering and development techniques ought to be further studied and experienced in order to define the evolutions to the data systems development process and framework to further develop the Aurora Avionics HW and SW elements introducing new technologies with an improved affordability and no compromise .to the overall quality levels.

Proposed way forward

In parallel to classical development on HW and SW technology at several levels (electronic design, mechanical, SW etc...), as well as the consolidation of on-board interface and services standardisation that have been identified within this study, the concept for future planetary exploration avionics systems would acquire a higher maturity level through an integrated modular avionics demonstration platform development that would be able to progressively integrate latest prototype development and support an end to end evaluation exercise. Such follow-on activity would demonstrate the ability of the concept to cope with several mission profiles and to be the backbone of a continuous step by step technology improvement process.

The starting point would be the A3SysDef assets from the functional architecture and the preliminary specification of HW and SW building blocks as well as from other technology improvement from recent other studies (Leon based SoC's, Mass Memory HW and SW elements,...). The baseline for this demonstration activity should make use of a consolidated CCSDS SOIS communication reference and include the selection and usage of adapted development, validation and simulation methods and tools. After the development and integration of a demonstration platform prototype based on generic requirements, two or more reference missions could be subject to a configuration and customisation exercise followed an evaluation of the data system properties, robustness and performance.

The practical experience of such development and the evaluation of the produced assembly of HW/SW prototype modules would fully demonstrate the suitability of the proposed approach and of the first implementation baseline to candidate projects such as ExoMars and Mars Sample Return. Moreover, such platform could also become a reference framework that would constitute a Data Processing and SW Development Environment able to support early assessment through fast configuration and prototyping activity for other candidate projects.